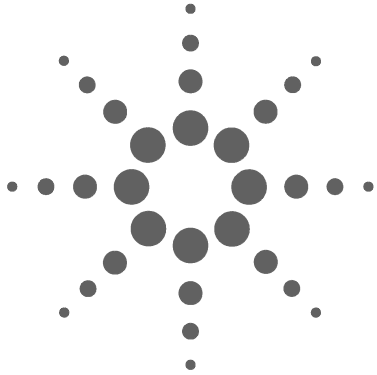


Agilent E8047A Analysis Probe System for the Intel® Xeon™ Processor Family

User's Guide

Agilent Technologies

Notices

Manual Part Number

E8048-97000

Print History

E8048-97000, February 2003

Agilent Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

Trademark Acknowledgements

UNIX is a registered trademark of the Open Group.

Windows and MS Windows are U.S. registered trademarks of Microsoft Corporation.

Windows NT is a U.S. registered trademark of Microsoft Corporation.

Warranty

The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Agilent disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Agilent shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Agilent and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a U.S. Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Agilent Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

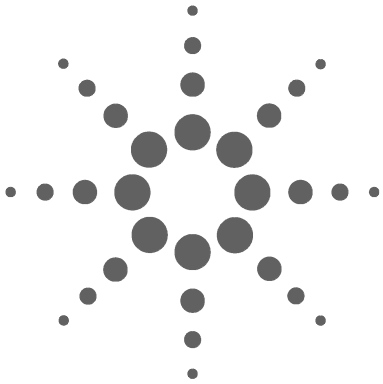
CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents



1
Equipment and Requirements

This chapter lists the equipment which is included with your analysis probe, and the additional equipment you need to make measurements.

In This Book

This book documents the following products:

- Agilent E8047A Analysis Probe for the Intel® Xeon™ Processor Family
- Agilent E8048A Interposer
- Software and Accessories

Equipment Supplied

This section lists equipment supplied with the analysis probe and equipment requirements for using the analysis probe.

The equipment supplied with the analysis probe is listed below:

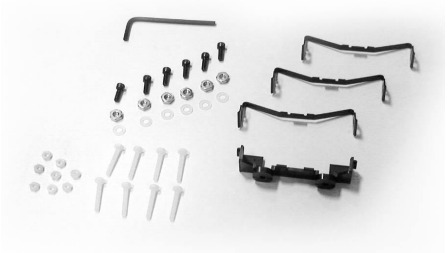
- E8047A analysis probe (often called a “logic analyzer interface” or LAI).
- Analysis probe cables, attached to the analysis probe.
- E8048A interposer.
- Pin protector. Leave this pin protector in place until you plug the interposer into the target system.
- Modified heatsink support and heatsink spring clips to support the heatsink when the interposer is in place. These clips have been modified to work with the Agilent interposer.
- Parts kit for attaching the heatsink, including nuts, screws, and a hex key. The kit also includes nylon hex screws and nuts for securing the analysis probe cables to the interposer. For your convenience, the kit contains extra quantities of some easy-to-misplace items.
- Cable ties, to help manage the analysis probe cables.
- Logic analyzer configuration files, and software on floppy disks or a CD-ROM.
- This *User’s Guide*.
- Power cord for the analysis probe.

  If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office. Use only the power cord supplied with the analysis probe.

See “To get replacement parts" on page 113 for a list part numbers.

E8047A
analysis probe

Power cord



Parts kit

E8048A
interposer

Additional equipment and software required

In addition to the items supplied with the analysis probe, you need all of the following items:

- An Agilent 16700-series logic analysis system. You may need to upgrade the operating system (see page 45) so that it has the same version number as the configuration files.
- Five Agilent 16753/4/5/6A logic analyzer modules
- A small, flat blade screwdriver (used to remove the heatsink spring clips).

Overview of Installation and Setup

CAUTION Read the instructions in this manual and in the online help before using the Probe Control Tool. For example, using the Debug Tab of the Probe Control Tool may cause loss of data or equipment damage.

NOTE Be sure to read all of the installation instructions, with special attention to the precautions required to prevent equipment damage. Note that this manual also contains instructions for disconnecting the equipment.

1. Check that you received all of the necessary equipment. See "Equipment and Requirements" on page 9
2. Prepare the target system and the space around the target system. See "Preparing the Target System" on page 17
3. Install logic analyzer modules in your logic analysis system, if necessary. See "Installing Logic Analyzer Modules" on page 43
4. Make the physical connections. This includes:
   - installing the interposer between the microprocessor and the socket on the target system,
   - connecting the analysis probe cables to the interposer, and
   - connecting the cables from the logic analyzer to the analysis probe.

   See the "Probing the Target System" chapter.
5. Turn on the logic analysis system.
6. Install the software. See "Installing Software" on page 45.

7 Turn on the analysis probe, then the target system. See “Power-ON/Power-OFF Sequence" on page 42

8 Load a configuration file. See “Loading Configuration Files" on page 50

9 Deskew the analyzer using the Probe Control Tool. See “Deskewing the logic analyzer" on page 52.

10 Begin making measurements.

Additional Information Sources

Additional or updated information can be found in the following places:

- The **online help** for the Probe Control Tool has information on deskewing and configuring the analysis probe. The help includes information about using the Probe Control Tool which does not appear in this manual.
- The **Installation Guide** for the interposer contains instructions which are the same as those which appear in the "Probing the Target System" chapter of this manual.
- Newer editions of this manual may be available. Contact your local Agilent representative.
- The **measurement examples** include valuable tips for making analysis measurements. You can find the measurement examples under the system help in your 16700-series logic analysis system.
- Your Agilent representative may have additional background information which can help you solve your test and measurement problems.

2
Preparing the Target System

This chapter describes the factors you need to consider when designing and preparing the target system for logic analysis with the analysis probe.

Mechanical Requirements

Keep-Out Area On the Target Board

The interposer extends slightly beyond the area normally occupied by the microprocessor. It is important to keep components from interfering with the interposer in this restricted area.

Figure 1 Keep-out area: interposer shadow as viewed from motherboard to bottom of interposer.

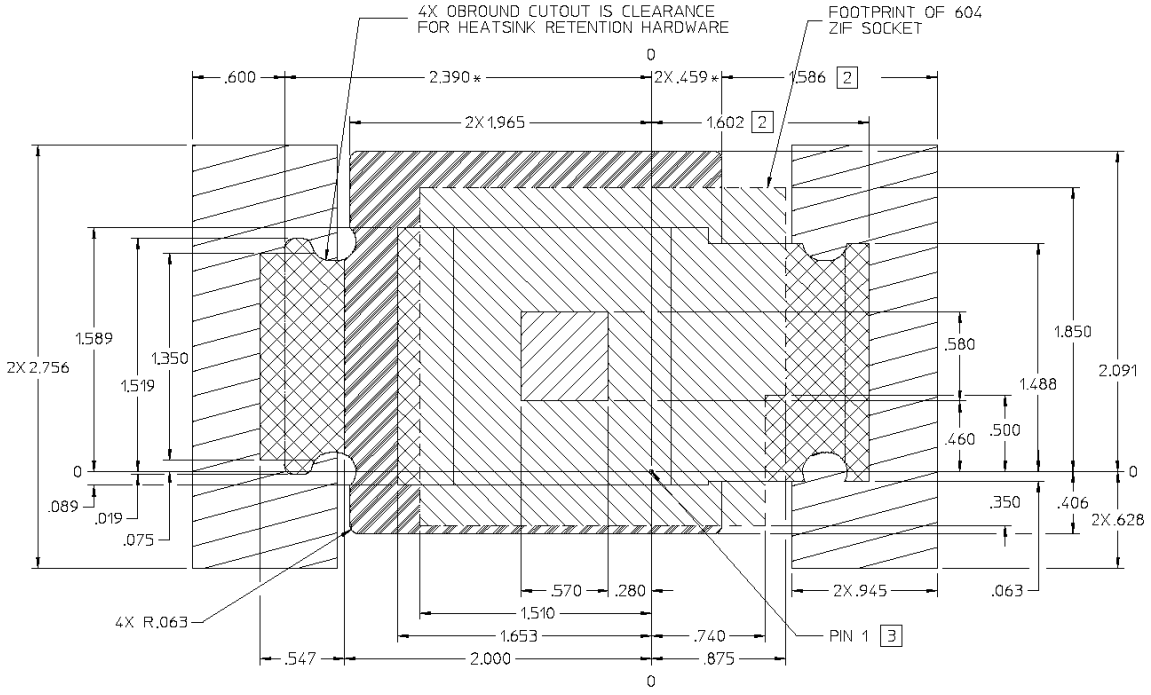


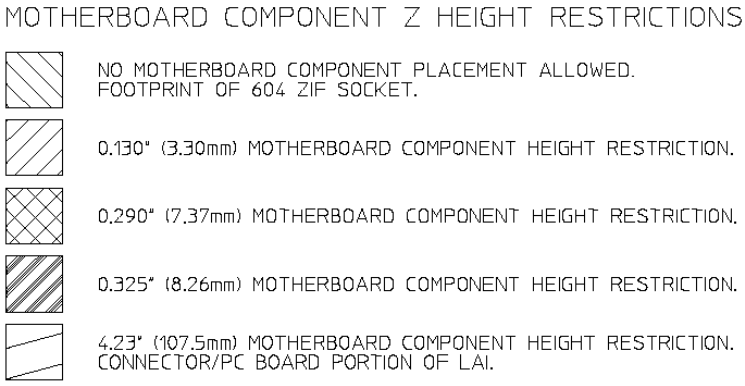
Figure 1 depicts the shadow that the interposer would cast on the target motherboard. The hatched regions indicate the maximum allowable height of components located on the socket side of the motherboard.

Notes:

***** Dimension indicates the edge of the rigid portion of the interposer.

2 Because the flexible portion of the interposer is routed under the heatsink retention hardware, the keep-out volume changes for those dimensions with alpha characters.

Figure 2 Maximum component heights for Figure 1

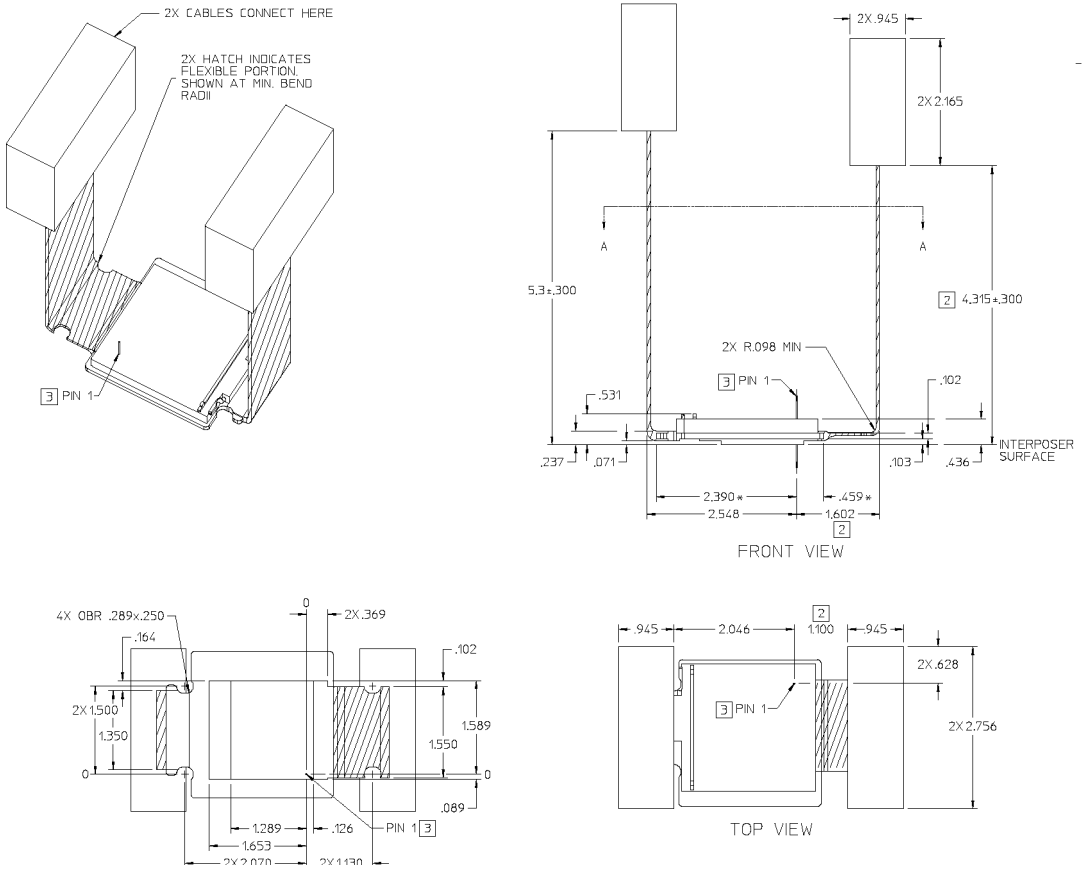


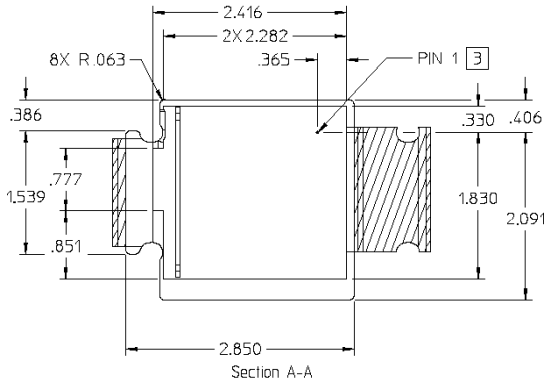
3 Reference is center of A1 pin recess in the socket, in the locked position.

Interposer Dimensions

The following illustration shows the approximate dimensions of the interposer. Design changes may result in slight variations from these dimensions.

Figure 3 Interposer dimensions





Socket

The top of the socket must be flat. If the socket on your target system has ridges, they need to be removed.

Clearance above the Target Board

Be careful to allow adequate space above the target board for the analysis probe, and for egress of the analysis probe cables.

The height of the paddles on the end of the interposer wings above the socket on the target system, without the analysis probe cables attached, is about 6.5 cm (about 3 inches).

CAUTION Allow enough room so that the interposer will not be twisted, pulled, or kinked during installation or use. See page 27 for a list of precautions to protect the interposer.

Heatsink Requirements

The interposer is shipped with modified heatsink retention hardware which is designed to work specifically with the Intel-recommended heatsink.

If you use a heatsink of your own design, pay close attention to the keep-out area requirements on the previous page.

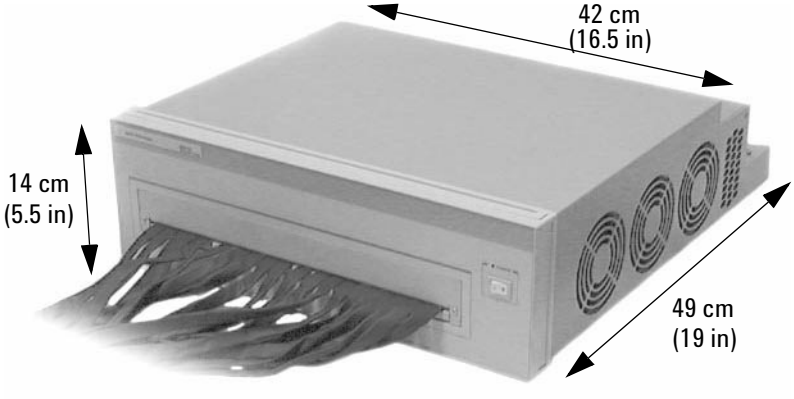
Bench Space for the Analysis Probe

Take care to allow space for the analysis probe be placed near the target system and the logic analysis system. You will also need plenty of space near the analysis probe for the logic analysis system and expander frame.

Allow at least 5 cm clearance on both sides of the analysis probe for proper cooling.

CAUTION Do not block the airflow holes on the sides of the analysis probe box. Blocked airflow may cause overheating and equipment damage

Figure 4 Analysis probe dimensions (approximate)



Target System Electrical Requirements

Unsupported positions

In a multiprocessor system, the analysis probe must be used in the end position farthest away from the chip set. Due to electrical requirements, the analysis probe cannot be used in the middle positions.

3
Probing the Target System

This chapter explains how to connect the Agilent E8048A interposer to the target system.

CAUTION To prevent equipment damage, remove power from the target system and analysis probe before making attachments.

NOTE Installation requires access to the back of the motherboard.

Protecting the Interposer

Here is a summary of precautions to take to avoid damaging the interposer:

DO minimize the removal of the analysis probe cables, once they are connected to the interposer.

DO minimize the removal of the interposer, once it is connected to the microprocessor and target system.

DO exercise patience and care when working with the interposer.

DO use ESD precautions.

DO remove power from the target system and analysis probe before making attachments.

DO protect the pins from damage by covering them with the pin protector when the interposer is not in use.

DO NOT insert any kind of tool between the interposer and the microprocessor, except as described in this manual.

DO NOT kink the analysis probe cables.

DO NOT pull on or twist the cables which are attached to the interposer.

Installing the Interposer with a Desktop Retention Mechanism

1 Gather the required parts:

- E8048A interposer

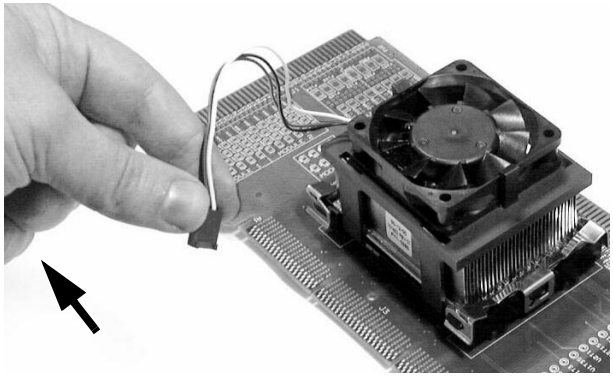
From the accessory kit supplied with the interposer:

- 2 nuts
- 2 metal screws
- 1 heatsink support (notice the deep cutout for the interposer cables)
- 2 heatsink spring clips (notice that they are taller than the normal clips, and lack the middle locking tab)
- 7/64 inch hex key

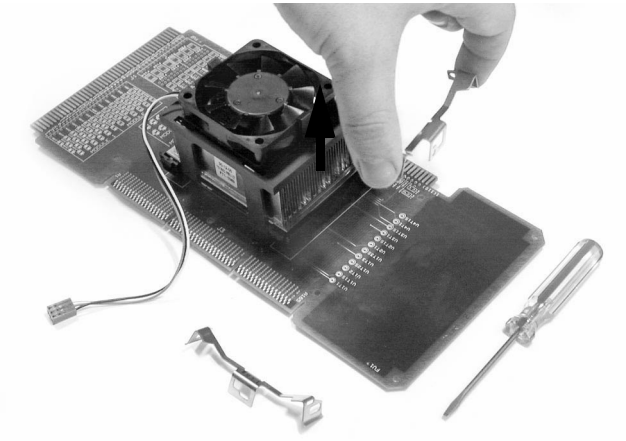
You may also need:

- A small flat-blade screwdriver (to remove the heatsink spring clips).
- Thermal paste (for reinstalling the heatsink).

2 Disconnect power from the fan.



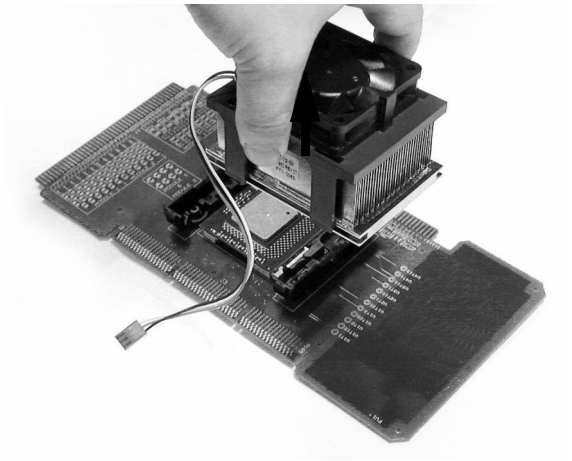
3 Remove the spring clips from the heatsink.



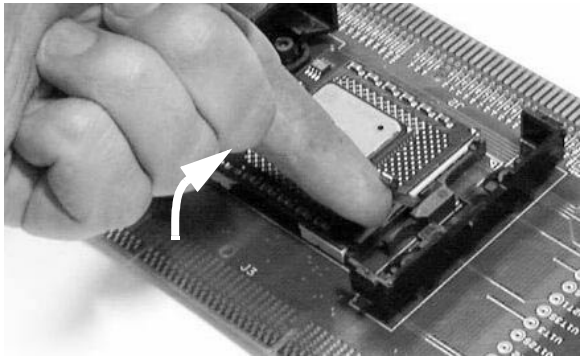
If necessary, cautiously use a small flat blade screwdriver to pry the clips away from the heatsink supports.

Set the clips aside in a safe place; you will not need them while the interposer is installed.

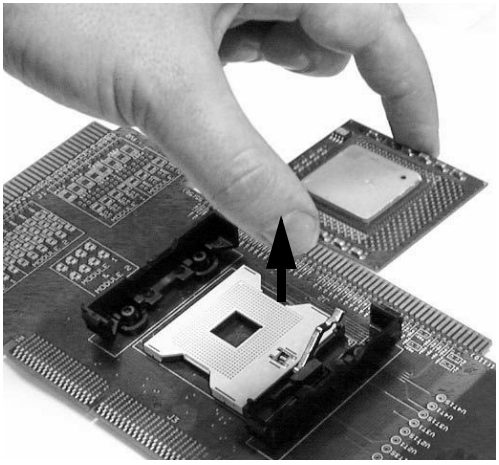
4 Remove the heatsink and fan from the microprocessor.



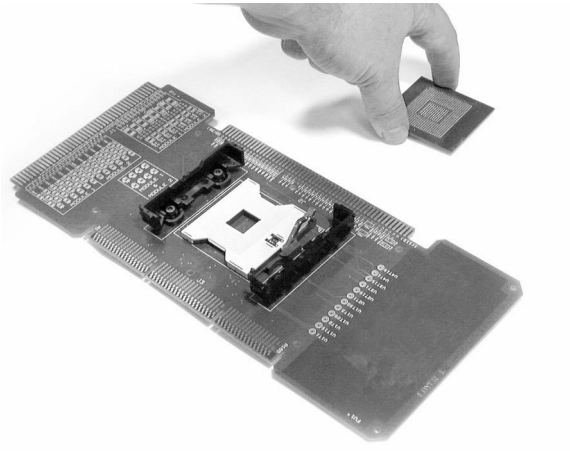
5 Open the socket on the motherboard.



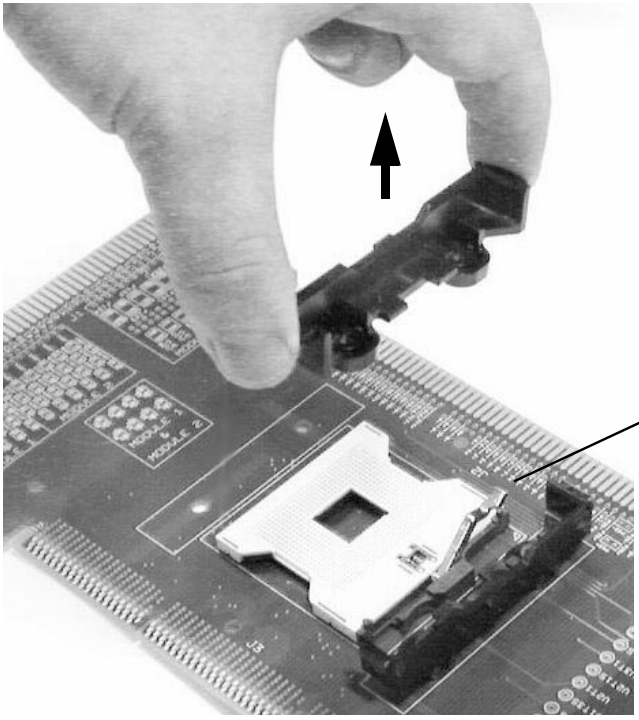
6 Remove the microprocessor from the motherboard.



7 Set the processor aside in a safe place, where nothing will bump it or damage the pins.



8 Remove the heatsink support which is opposite the lever on the motherboard socket.

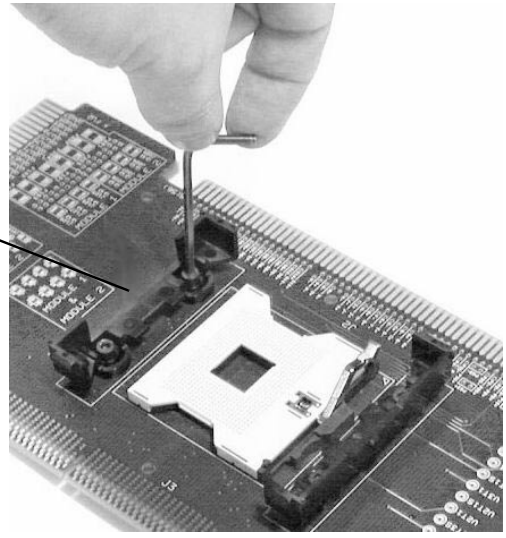


To remove the heatsink support, you need to have access to the back side of the motherboard.

Put the fasteners and heatsink support aside in a safe place.

9 Install the supplied heatsink support on the motherboard.

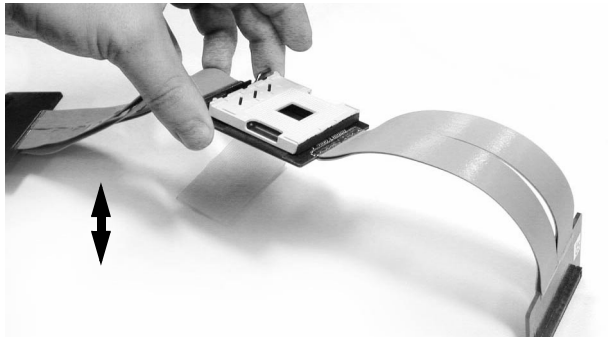
If the original fasteners don't work, use the supplied metal screws and nuts to attach the heatsink support.



10 Check that the socket on the motherboard is open.

11 Remove the pin protector from the interposer.

Keep the pin protector. You will need it to prevent damage to the interposer whenever the interposer is not plugged into the target system.

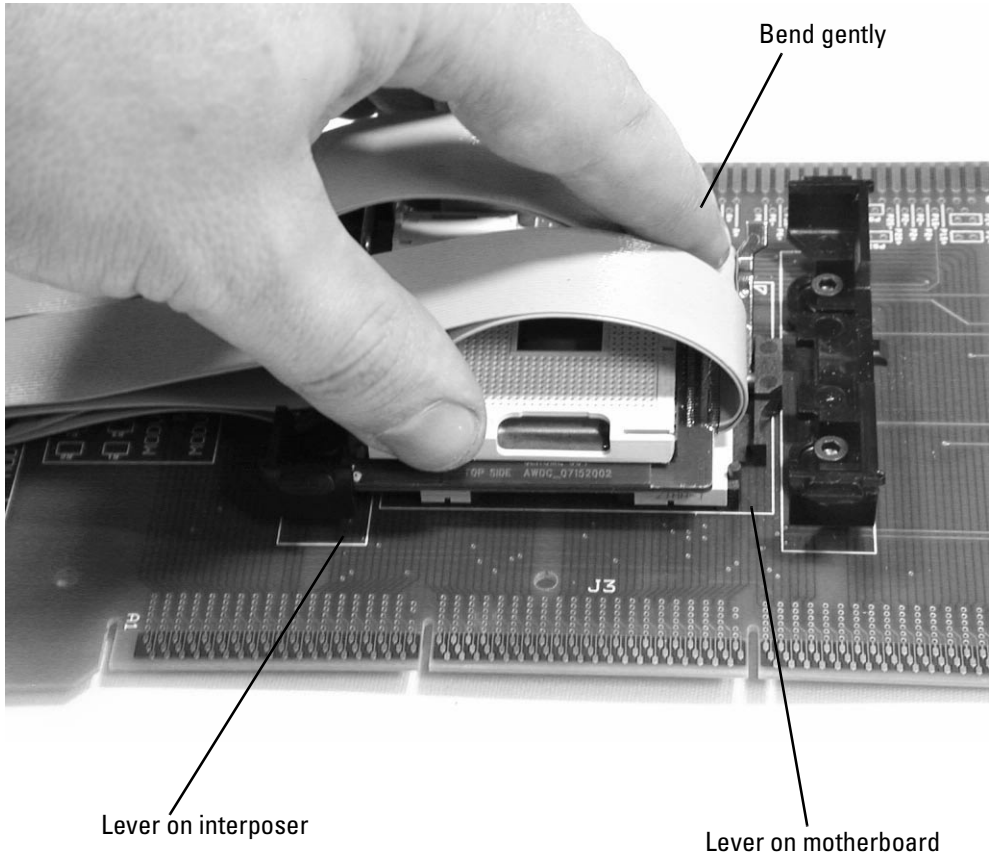


12 Align the interposer over the socket on the target system.

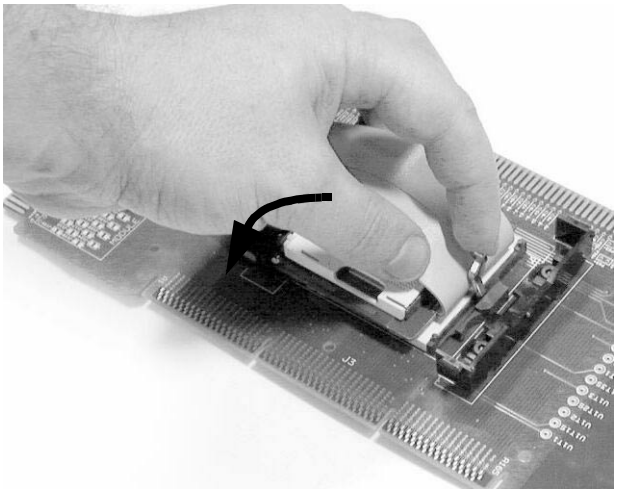
Note how the socket on the interposer is rotated 180° relative to the socket on the target system.

Gently bend the interposer cables back, so that they do not interfere with the lever of the socket on the motherboard. Do not kink or crease the cables.

Gently align the assembly until you feel the pins fall into the holes of the socket.



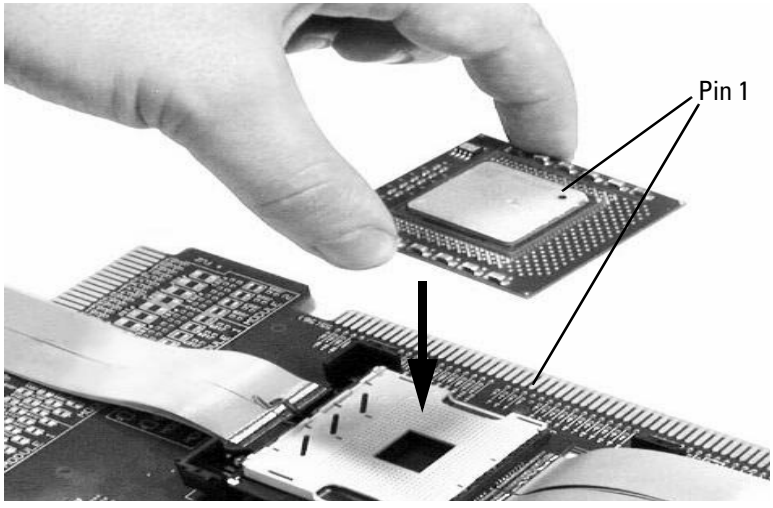
13 Close the socket on the motherboard.

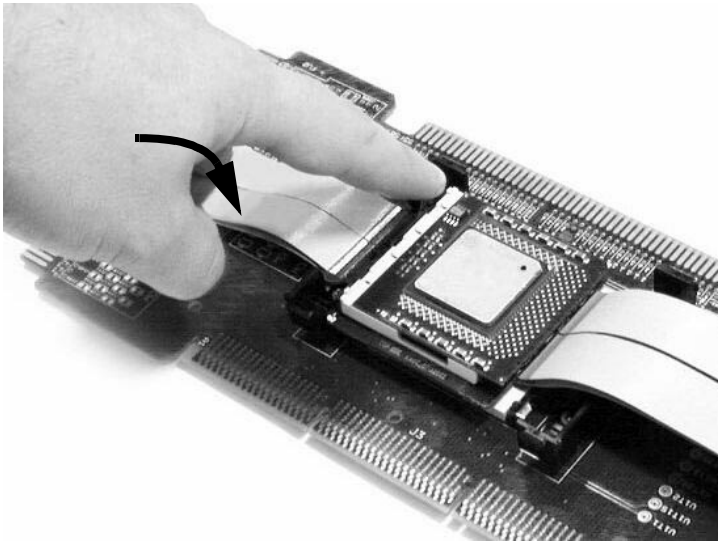


If necessary, use one hand to hold the interposer flat against the socket.

14 Check that the socket on the interposer is open.

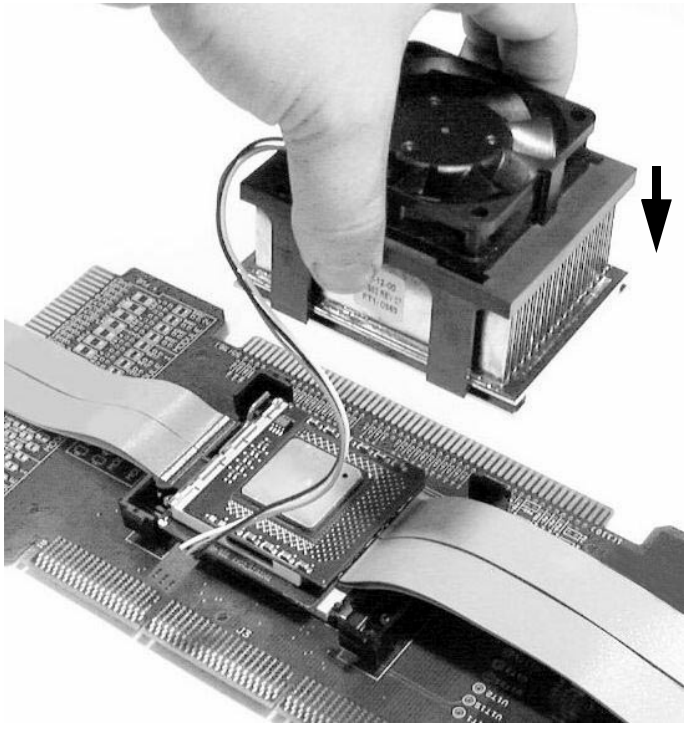
15 Align the processor over the socket on the interposer. Gently align the processor with the socket until you feel the pins fall into the holes. Visually check that the bottom of the processor is flush with the top of the socket on the interposer, then close the socket.



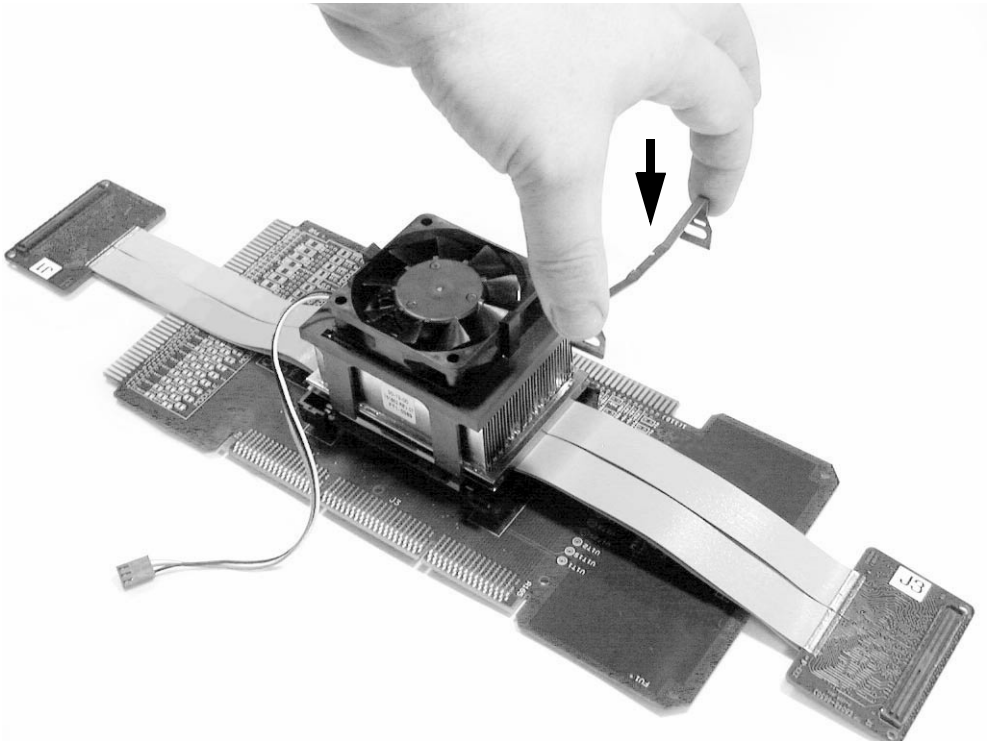


CAUTION Note that the orientation of the processor with respect to the interposer socket is opposite from the target system. A dot on the interposer indicates the position of pin A1.

16 Apply thermal paste and set the heatsink on the processor.



17 Install the supplied heatsink spring clips.



18 Reconnect power to the fan.

19 Connect the analysis probe cables to the interposer.

Refer to the silkscreened labels on the interposer and on the cable paddles. Be careful to plug the cables straight in, without any rocking motion.

20 Optional: install the supplied nylon screws to keep the paddles on the end of the analysis probe cables from pulling apart.

21 Connect the analysis probe to the logic analyzer.

Connect the pod cables to the connectors on the analysis probe as shown on the back of the analysis probe.

Uninstalling the analysis probe

CAUTION To maximize the life of the interposer and socket, minimize uninstalling and reinstalling the interposer.

CAUTION If possible, leave the analysis probe cables attached to the interposer.

CAUTION Use ESD precautions. Electrostatic discharge (ESD) can damage the interposer, as well as the target system. Use grounded wrist straps and mats when you handle the interposer.

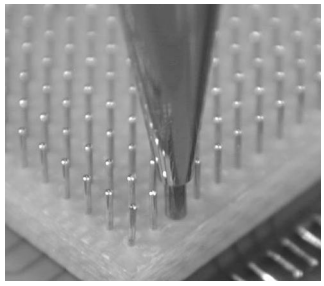
1. Remove power from the target system and from the analysis probe.

   You may leave the logic analysis system turned on.
2. Remove the heatsink.
3. Remove the processor from the interposer.
4. Remove the interposer from the target system.
5. Remove the retention module frame.
6. Re-install the processor on the target system.
7. Re-install the heatsink.

To straighten bent pins

When handling or installing the processor or the interposer, care must be taken not to bend pins. Here is a practical suggestion for straightening bent pins:

1. Find a 0.5mm mechanical pencil.
2. Remove the lead from the tip of the pencil.
3. Place the tip of the pencil over the bent pin and bend it to the correct angle.



If a pin on the interposer breaks

Broken pins cannot be repaired.

If only one pin (or a few pins) on the interposer is broken, check whether the pin carries a signal which you need to capture. If the pin is a ground or power pin, measurements should not be affected.

To find out whether the broken pin is an "important" one, consult your pinout documentation for the processor.

4
Setting Up the Logic Analysis System

This chapter shows you how to power on the logic analysis system, how to set up the logic analyzer modules, and how to install the software.

Power-ON/Power-OFF Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

Use only the power cord supplied with the analysis probe.

To power-ON

Ensure the target system is powered off.

1. Turn on the logic analysis system.
2. Turn on the analysis probe.
3. Configure the logic analysis system. See “Configuring the Logic Analysis System" on page 49.
4. When the logic analysis system is connected to the target system, and everything is configured, turn on your target system.

To power-OFF

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off the analysis probe.
3. Turn off your logic analysis system.

To cycle power on the target system

- Cycle power on the target system only. You do not need to turn off the analysis probe or logic analysis system.

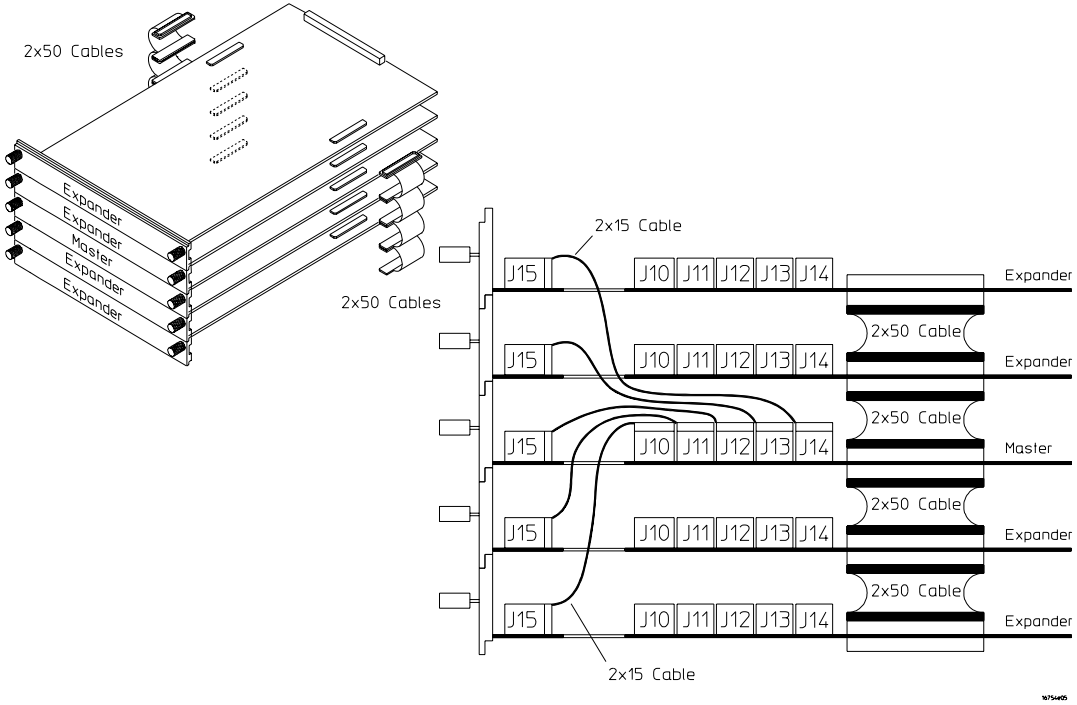
Installing Logic Analyzer Modules

You should install logic analyzer modules in your logic analysis system before you begin make connections or configure the logic analysis system.

Five logic analyzer cards in the logic analysis system must be connected together as one machine. Connect the cards so that the master card is in slot C (or slot H in an expander frame).

Use five 2 x 15 cables and eight 2 x 50 cables (in the accessory pouch) to connect the modules

NOTE Turn off the mainframe power before removing, replacing, or installing modules.



All of the cards machine should be of the same type.

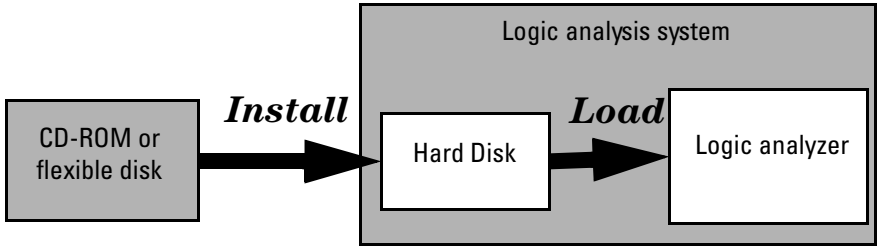
Refer to the Agilent 16700-series logic analysis system's *Installation Guide* for more information on how to install the cards and connect them together.

Installing Software

This section explains how to install the software you will need for your analysis probe.

Installing and loading

Installing the software will copy the files to the hard disk of your logic analysis system. Later, you will need to load some of the files into the logic analyzer module.



What needs to be installed

Install the following software from the provided floppy disks or CD-ROMs:

1. Logic analysis system operating system patches, if applicable.
2. Logic analysis system configuration files.

NOTE

Install the disks in the order listed above.

The version number of the operating system must match the version number of the configuration files.

The logic analysis system will end the current session after installing the patch and again after installing the configuration files.

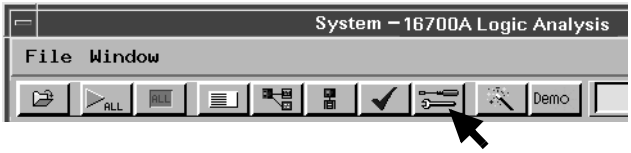
Installing the configuration files also installs the Probe Control Tool software.

To install software from floppy disk

Installing a processor support package will take just a few minutes.

1 Insert the first disk in the drive.

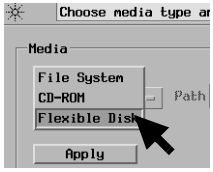
2 Select the **System Admin** icon.



3 Select the **Software Install** tab.

4 Select **Install...** .

Change the media type to “Floppy Disk” if necessary.



5 Select **Apply**.

6 Select the *E8047A Preprocessor* software package.

If you are installing from a floppy disk,only one package will be listed.

7 Select **Install**.

The Continue dialog box will appear.

8 Select **Continue**.

The dialog box will display “Progress: completed successfully” when the installation is complete.

9 If required, the system will automatically reboot. Otherwise, close the software installation windows.

The configuration files are stored in */logic/configs/hp/E8047A*.

The inverse assembler is stored in */logic/ia*.

See the on-line help for more information on installing, licensing, and removing software.

5
Configuring the Logic Analysis System

This chapter shows you how to load configuration files, which set up the logic analysis system for your microprocessor, and how to further configure the software before you begin making measurements.

Loading Configuration Files

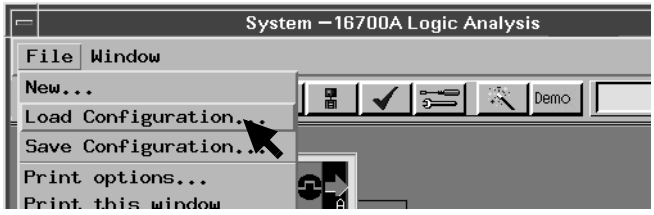
The first step in configuring the logic analyzer is loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer.
- Settings for State or Timing modes.

There are two configuration files: one for the State modes and one for Timing mode.

To load configuration files

1 In the System window, select the Load Configuration... command from the File menu.



2 In the File Manager dialog, browse to the **/logic/configs/hp/E8047A** directory

If this directory does not exist, see "To install software from floppy disk" on page 46.

3 Using File Manager, select the configuration file from the configuration file directory, then click Load.

Load **E8047_state.___** for state mode (synchronous measurements).

Load **E8047_timing.___** for timing mode.

4 Close File Manager.

When you load a configuration file, the following things happen:

- The workspace is set up.
- The state (synchronous) or timing sampling mode is selected.

- Buses and signals coming from the analysis probe to logic analyzer channels are mapped to labels.
- Logic analyzer pod threshold voltages are set.
- If the configuration was originally saved “with data,” then Eye Finder data is loaded.

NOTE You must set up the sampling mode and analyzer labels by loading a system configuration file. Do not attempt to change between state and timing mode without loading the appropriate configuration, because the logic analyzer labels are different in these two modes.

The version number of the configuration file must match the version number of the logic analysis system’s operating system.

To create your own configuration files

If you create and save your own configurations, start with a copy the supplied configuration file and delete the labels you don’t need, rather than building a configuration from scratch.

There are some characteristics of the supplied configuration file that you should be aware of:

- The data bus is split between four labels. The upper and lower 32 bits are split (this is necessary because the logic analyzer allows only 32 bits to be assigned to a label). Quad pumped data is reduced to double pumped. P strobe data is labeled _1 and N strobe data is labeled _2.
- To save a configuration, be sure to save the whole workspace, not just the logic analyzer configuration.

See the online help in any logic analysis system window for general information on modifying, saving, and loading configuration files.

Deskewing the logic analyzer

You must deskew the analyzer before running any state mode measurements. Deskewing trains the logic analyzer to sample each signal at the moment that it is most likely to be stable.

To deskew the analyzer, use the Probe Control Tool. More information on deskewing can be found by selecting Help > On this window from the Probe Control Tool.

When to deskew the analyzer

Deskew the analyzer when:

- Any of the logic analyzer modules in the logic analysis system are replaced.
- Changes are made to the analysis probe or to the logic analyzer modules.
- The temperature is changed significantly.
- The frequency of the front-side bus being probed is changed to a frequency which is higher than what was used to deskew the analyzer.
- The analyzer mode is changed between Timing and State. (Reminder: to change between Timing and State modes, you must load the appropriate configuration file.) If you have saved Eye Finder data for the analyzer mode, you may reload that data instead of deskewing again.
- The analysis probe is connected to a new target system.

To prepare to deskew

1. Make sure the analysis probe is connected to the interposer.
2. Make sure the interposer is connected to the target system.
3. Make sure the analysis probe is connected to the logic analysis system.
4. Make sure the analysis probe and target system are both turned on.

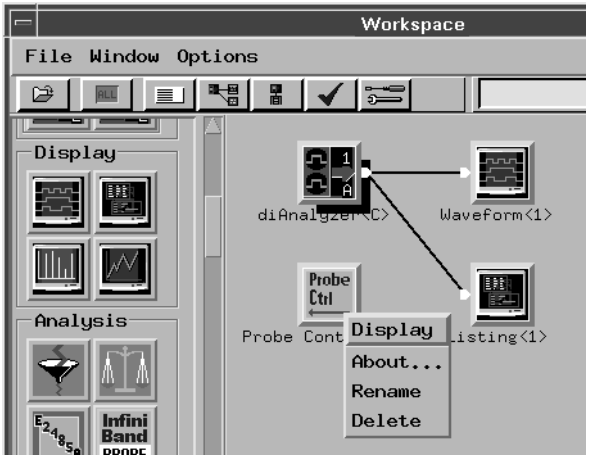
5 Make sure the target system is in a mode where it is supplying the BCLK signal. If your target has the ability to generate BCLK at different frequencies, it is recommended that you use the highest frequency (up to 200 MHz) for deskewing.

To start the Probe Control Tool

1 Display the Workspace window.

2 Loading one of the provided configuration files places a Probe Control Tool on the workspace. If the tool was removed from the workspace, drag a Probe Control Tool onto the workspace.

3 Open the Probe Control Tool.



If a single analysis probe is connected

When you select the *Connect* tab, the source will be highlighted on the list and the *Select Source* button will already be selected.

If several analysis probes are connected

1 Select the *Connect* tab.

2 Select which analysis probe you want to set up using the Probe Control Tool.

3 Select *Select Source*.

If no analysis probes are displayed

If no analysis probes are displayed on the Connect tab:

1 Check that the analysis probe is physically connected to the logic analysis system.

2 Check that the analysis probe is powered on.

3 Run the target so that it is supplying BCLK. Go to the Format tab of the analyzer and look for activity on clk C[J]. Activity on this signal is a good indication that the logic analyzer cables and interposer cables *are* correctly connected. (Note that the opposite does not hold true: it is possible that BCLK will not be detected because the Probe Control Tool has not yet set up the comparators in the analysis probe.)

4 Select *Search Source*.

The Probe Control Tool does not need to be connected to any other tools in the workspace.

CAUTION Read the instructions in this manual and in the online help before using other tabs of the Probe Control Tool. For example, using the Debug Tab of the Probe Control Tool may cause loss of data or equipment damage.

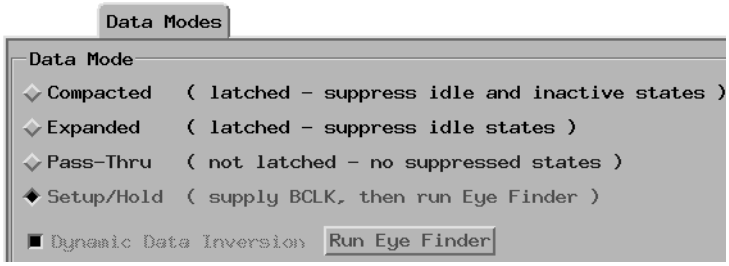
To begin the deskewing process

1 Make sure that a BCLK signal is being provided from the target system (see "To prepare to deskew" on page 52).

2 Open the Probe Control Tool.

3 Select the *Data Modes* tab.

4 Select the *Setup/Hold* mode.



This step enables the Run Eye Finder button.

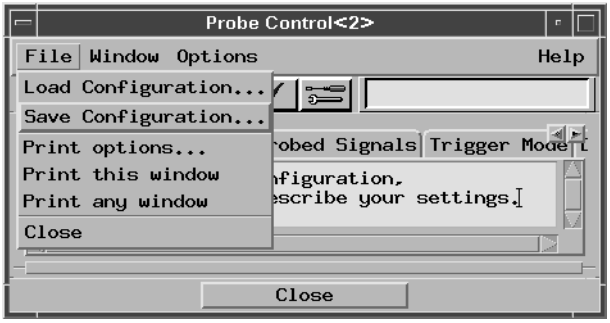
5 Select *Run Eye Finder*. It takes about 15-20 minutes to deskew the analyzer. Progress is displayed in the Eye Finder results window.

6 Save the Eye Finder data.

To save settings and Eye Finder data

To save Probe Control Tool settings

1. (Optional) Enter a description of the current set-up in the Comments tab of the Probe Control Tool. It is often helpful to include information (such as serial numbers) which can uniquely identify the logic analyzer, analysis probe, interposer, and target system for which the configuration is valid.
2. Save a configuration, using the File menu of any tool in the workspace.

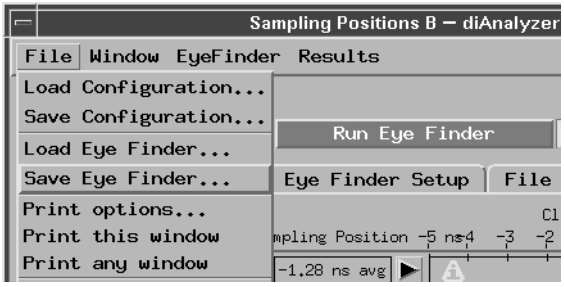


The configuration file will include any changes you have made from the supplied configuration file, including:

- Changes to the workspace.
- Changes to labels in logic analyzer machine or in any of the display tools.
- Changes to settings in the Probe Control Tool.

To save Eye Finder data

- In the Eye Finder (that is, in the Sampling Positions dialog) use the File menu to save the results of the deskewing process.



Choose a file name which specifies the bus frequency and the analyzer setup.

It is a good idea to save Eye Finder data *immediately* after deskewing the analyzer and verifying the results.

To load Eye Finder data

Load Eye Finder data after you have loaded a new state configuration file.

NOTE

Each Eye Finder data file is specific to the logic analysis system setup which was used for the deskewing run. If the hardware setup has changed in any way (see "When to deskew the analyzer" on page 52) then you should deskew again.

1. Open the logic analyzer's Sampling tab.
2. Select Sampling Positions....
3. Select File then Load Eye Finder....
4. Select the file to load.

See "Deskewing the logic analyzer" on page 52 for more information on deskewing.

See the Help menu in the Sampling Positions dialog for more information about Eye Finder data files.

Loading Symbol Information

Symbols are more easily recognized than hexadecimal address values in logic analyzer trace displays, and they are easier to remember when setting up triggers.

Agilent logic analyzers let you assign user-defined symbol names to particular label values.

Also, you can download symbols from certain object file formats into Agilent logic analyzers.

To view predefined symbols

User-defined symbols are symbols you create in the logic analyzer by assigning symbol names to label values. Typically, you assign symbol names to address label values, but you can define symbols for data, status, or other label values as well.

User-defined symbols are saved with logic analyzer configurations. The supplied logic analyzer configuration files contain predefined symbols for logic analyzer labels.

To display the predefined symbols:

1. Open the logic analyzer's Setup window.
2. Select the Symbols tab.
3. Select the User Defined Symbols tab.
4. Choose a label name from the "Label" list.

   The logic analyzer will display the symbols associated with the label.

To load object file symbols

The most common way to load program symbols into the logic analyzer is from an object file that is created when the program is compiled. The object file containing symbolic debug information must be in a format the logic analyzer understands.

If your compiler generates object files in a format that the logic analyzer doesn't understand, you can use a General-Purpose ASCII (GPA) symbol file (see "General-Purpose ASCII (GPA) Symbol File Format" on page 103).

To load symbols in the Agilent 16700-series logic analysis system:

1. Open the logic analyzer module's Setup window.
2. Click the Symbol tab.
3. Click the Object File tab.

   Make sure the label is ADDR.

From this dialog you can select object files and load their symbol information.

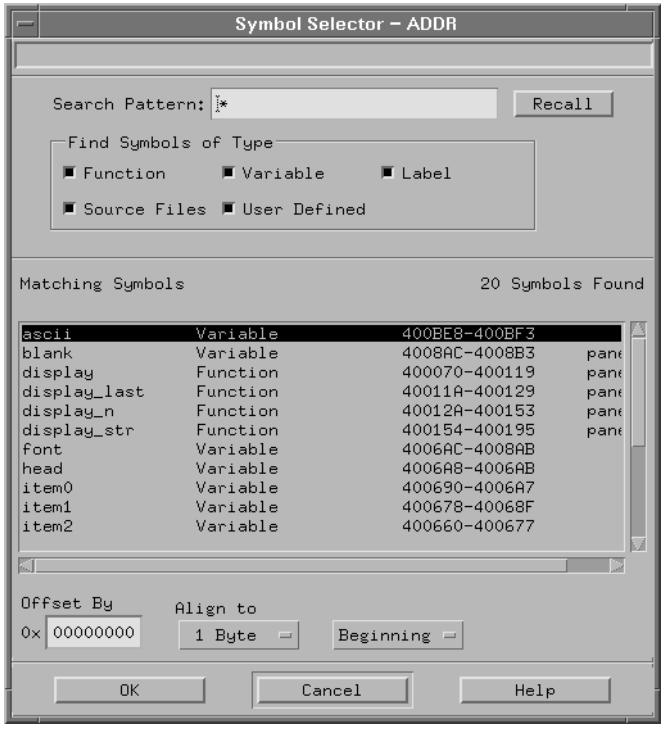
When you load object file symbols into a logic analyzer, a database of symbol/line number to address assignments is generated from the object file.

To access the Symbol Selector dialog

The Symbol Selector dialog allows you to view the database so you can find a symbol to use in place of a hexadecimal value when defining trigger patterns, trigger ranges, and so on.

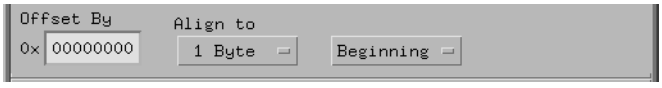
The Symbol Selector dialog may be accessed in various ways. One way to access the Symbol Selector dialog is from the Search tab in the Listing display.

1. Under the Search tab in the Listing display, click Advanced Searching.
2. In the Goto Pattern dialog, click Define.
3. In the Search Pattern dialog, select the Symbols numeric base.
4. Select Pattern, Range, Not Pattern, or Not Range.
5. Click the field to the right of the Pattern/Range selection button.
6. In the Symbol Selector dialog that appears, select the symbol you want to use.



To compensate for relocated code

When code segments are relocated, or when memory management units produce fixed code offsets, you can compensate by using the address offset field in the Symbol Selector dialog.



Entering the appropriate address offset will cause the logic analyzer to reference the correct symbol information for the relocatable or offset code.

Setting Up Labels for Groups of Signals

Predefined Label Descriptions

The logic analyzer configuration file automatically sets up labels for most microprocessor signals.

Labels which correspond to processor signals are displayed in upper case.

Labels which for signals which are generated by the analysis probe are generally displayed in lower case.

For a list of all of the signals, see “Signal-to-connector mapping" on page 91.

To define additional labels

1. Open the Setup window.
2. Click the Format tab.
3. Click a label and select Insert before... or Insert after....
4. Click the signals under the appropriate pod, then select which bits to include in the label.

Configuring Signal Thresholds

CAUTION

Do not change the signal thresholds or set-up and hold times.

Remember that the logic analyzer is connected to the analysis probe. Changing these parameters will only disrupt the communication between the analysis probe and the logic analyzer—it will not affect how the analysis probe acquires signals from the processor.

6
Capturing Execution

This chapter shows you how to set up logic analyzer triggers to capture just the data you want.

The normal steps in using the logic analyzer are:

1. Configure the logic analyzer.
2. Load symbols from the program's object file.
3. Set up the trigger, and run the measurement.
4. Display the captured data.

The logic analyzer is configured, and labels are created (formatted) for the logic analysis channels when configuration files are loaded (see "Loading Configuration Files" on page 50).

You can load program object file symbols into the logic analyzer when configuring it (see "Loading Configuration Files" on page 50).

This chapter describes setting up logic analyzer triggers. See "Displaying Captured States" on page 71 for information on displaying captured data.

NOTE

Note: The screens you see may be different from what you see in this manual, depending on the version of your logic analyzer system software.

State and Timing Modes

You can capture data in state mode (where data is sampled sychronously with BCLK) or in timing mode (where data is sampled asynchronously and you can see the timing relationships between signals).

NOTE **You *must* set up the sampling mode and analyzer labels by loading a system configuration file.** Do not attempt to change between state and timing mode without loading the appropriate configuration file (E8047_timing.___ or E8047_state.___), because the logic analyzer labels are different in these two modes.

NOTE **You *must* deskew the analyzer before capturing data in state mode.** You can either use the Probe Control Tool to deskew the analyzer, or load previously saved Eye Finder data. See "Deskewing the logic analyzer" on page 52.

Choosing Which States to Store

In state mode, you can control how much data is captured by the analyzer, and make the listing display easier to read, by using storage qualification to store only selected kinds of states.

Storage qualification acts as a real-time filter which allow you to selectively remove idle states and snoop stalls from the captured data. For uses such as BIOS debug, removing idles and snoop stalls provide a more compact and readable view of the bus to optimize the capture of pertinent data in the trace memory of the analyzer.

Storage qualification can be set up using a combination of:

- The settings under the Data Mode tab, and
- The default storing configuration in the logic analyzer's Setup window.

To store all states

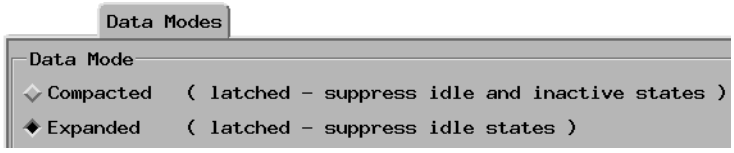
Also known as "All" mode.

1. Open the Probe Control Tool and select the Data Mode tab.
2. Select either Compacted or Expanded.
3. Open the Setup window.
4. Select the Trigger tab.
5. Select the Default Storing tab.
6. Set Store by default to Custom, and set storage qualification to "Anything".

To store all except idle states

Also known as "Expanded" mode. This mode stores states whenever a bus cycle is active, the data bus is active, BINIT# is active a Reset is active, and two BCLK states after Reset.

1. Open the Probe Control Tool and select the Data Mode tab.
2. Select Expanded.



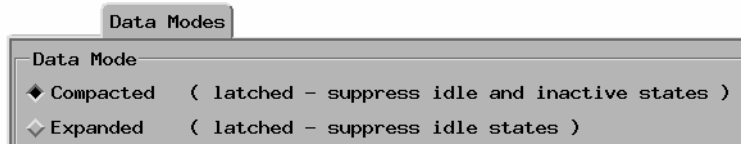
3. Open the Setup window.
4. Select the Trigger tab.
5. Select the Default Storing tab.
6. Set Store by default to Custom, and set storage qualification to "Store if Cqual# = 0".

To store all except idle and inactive states

Also known as "Compacted" mode. This mode stores the same states as Expanded mode, except for consecutive reset states, consecutive snoop stalls, and states where the data bus is active but no data is being transferred. This is the default mode.

1 Open the Probe Control Tool and select the Data Mode tab.

2 Select Compacted.



3 Open the Setup window.

4 Select the Trigger tab.

5 Select the Default Storing tab.

6 Set Store by default to Custom, and set storage qualification to "Store if Cqual# = 0".

To use timing mode (Pass-Thru mode)

1 If you have already deskewed the analyzer, make sure that you have saved the Eye Finder data. If the Eye Finder data is not saved, you will need to deskew the analysis probe again when you go back to State mode.

2 Load the Timing configuration file (E8047_timing.___ or another system configuration file which you have saved based on this file).

NOTE Do not try to enable timing mode just by selecting the Pass-Thru data mode. Instead, you must load a Timing configuration file, which will change the analyzer mode to Timing mode, change the analysis probe mode to Pass-Thru, *and* change the signal mappings.

Other modes

The Setup/Hold mode is used to deskew the analyzer.

See also “Dynamic Data Inversion” in the Probe Control Tool online help.

When to use the Trigger Mode tab

In most cases, you will not need to make any changes under this tab.

The Trigger Mode tab of the Probe Control Tool lets you add additional data labels which can be used by logic analyzer triggers in state mode.

Always select Modified General State mode (this is the default).

The data labels (Dxx and DBIx) are selected by default. Do not delete them.

Add additional labels here if:

- You have defined a new label for some data signals, AND
- The new label does not use the same signals as any label set up by the configuration file, AND
- You want to use the new label in a trigger.

When to use the Sampling tab

You may safely use the Sampling tab of the logic analyzer’s Setup and Trigger window to change:

- Trigger position (start/center/end)
- Sampling positions (after deskewing, to “fine-tune” the results if necessary)
- Acquisition speed/depth

Many of the settings are set by the configuration files and should not be modified. *Do not* use the Sampling tab to change:

- Analyzer mode (state/timing/eye scan)
- Clock setup

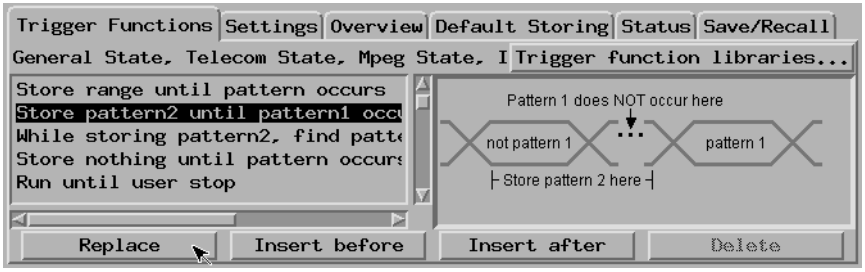
Setting Up Logic Analyzer Triggers

To set up logic analyzer triggers

1 Open the logic analyzer's Setup window.

2 Select the Trigger tab.

3 Select the trigger function that will be used in the logic analysis measurement and press the Replace button.



4 Define the patterns, ranges, and other resources that will be used in the logic analysis measurement.

5 Run the measurement.

Refer to the online help for the Probe Control Tool for information about triggering on data labels which you have added.

Refer to the Agilent 16700-series logic analysis system's on-line help for general information on setting up logic analyzer triggers.

Triggering on a transaction type

Triggering on address and transaction type

To trigger on a specific address and transaction type, use the A35-32, A31-00, and TranTy labels, together with the TranTy label symbols. The symbols identify each transaction type uniquely, except for Interrupt Acknowledge and Special Transactions, which are combined into one symbol.

Triggering on data and transaction type

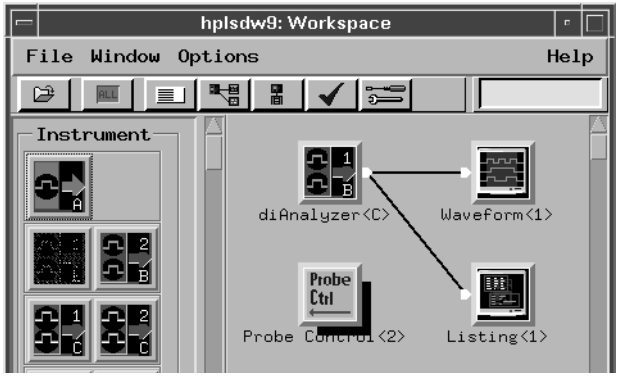
There is no guaranteed method of triggering on a particular transaction type or address ANDed with a particular data value in a target system with overlapping transactions. Alignment in the Listing window is the result of post-processing and cannot be used for triggering. The analysis probe hardware captures this information on different states. A trigger specification could be defined to find a certain transaction type; however, by the time the data pattern is found, it could belong to a different transaction.

7
Displaying Captured States

This chapter shows how to display, filter, and interpret data which has been captured by the logic analysis system.

Understanding the workspace

The Workspace window shows the relationship between the parts of your measurement setup:



Data labels

There are two sets of data labels. Labels are limited to 32 bits, so there are a total of four data labels.

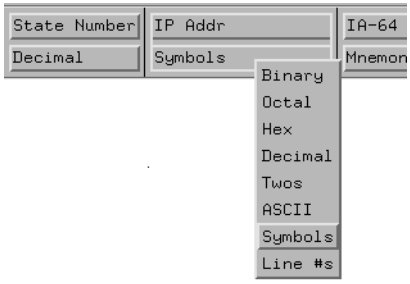
To display the captured data

1 In the Workspace window, connect a Listing display to the output of the analyzer.

See the Agilent 16700-series logic analysis system on-line help for information on using the Listing display.

To display symbols

- In the Listing window, select the label base and select Symbols.



You can display a label in symbolic form, if you have defined symbols for that label. Any symbols that have been defined will be displayed in place of the captured values.

For example, if your compiler or assembler outputs a symbol file, you can display IP addresses in terms of the modules and functions in your source code.

See also "Loading Symbol Information" on page 58 and "Loading Configuration Files" on page 50.

Displaying Signals as Waveforms

To display timing information

To capture these waveforms:

1. Load the Timing configuration file.
2. In the Workspace window, connect a Waveform tool to the output of the logic analyer tool, as shown on page 71.

You can also use the Waveform display in the state analysis mode to display state timing diagrams.

Using Dynamic Data Inversion

To reduce noise on the data bus, the processor selectively inverts groups of 16 bits. An inversion status bit is associated with each group of 16 bits to indicate whether that group was inverted.

Manually interpreting this data can be cumbersome. As a convenience, the analysis probe un-inverts the inverted data *before sending it to the logic analyzer*, so all data appears logically true. This is called dynamic data inversion.

To use dynamic data inversion on the data bus

Dynamic data inversion is enabled by default.

1. Open the Probe Control Tool.
2. Select the Data Modes tab.
3. Select Dynamic Data Inversion.
4. Run the measurement.

The advantage of dynamic data inversion is that *all* data will be displayed in its logically true form. The disadvantages of dynamic data inversion are that you will see apparent parity errors (parity calculations include the inversion bits) and that the inversion bits will all appear as 0, regardless of their actual value on the bus.

To disable dynamic data inversion

1. Open the Probe Control Tool.
2. Select the Data Modes tab.
3. Unselect Dynamic Data Inversion.

Disable dynamic data inversion if you want to see the data signals as they physically appear on the bus, or if you are using software to post-process the listing, and the software uses the inversion bits.

Using Other Tools to Process and Display Your Data

Useful tools

Some tools in your logic analysis system which are useful for analysis of IA-32 processors include:

Chart Tool

For displaying x-y plots of various data values.

Compare Tool

For comparing a "golden trace" from a known-good target system to a trace from another target system.

Distribution Tool

For displaying an overview of activity in a bar-graph form.

Pattern Filter

For excluding selected data from a data stream before you view it or store it.

System Performance Analyzer

(Licensed separately.) For displaying the distribution of bus events in time, for visually identifying patterns of activity, and for identifying operations which consume significant system resources.

Tool Development Kit

(Licensed separately.) For writing programs to postprocess data in any way you like.

8
Troubleshooting the Analysis Probe

This chapter explains how to solve problems you could encounter when you use the analysis probe.

If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent Technologies service center.

CAUTION When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, the interposer, or the analysis probe. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Logic Analyzer Problems

This section lists general problems that you might encounter while using the logic analyzer.

Intermittent data errors

Intermittent data errors are usually caused by incorrect sampling positions. To set the sampling positions:

- ✔ Deskew the analyzer. See “Deskewing the logic analyzer" on page 52, or
- ✔ If you have saved eye finder data after deskewing the analyzer, and the setup hasn’t changed, load the eye finder data file. See “To load Eye Finder data" on page 57.

This problem is can also be caused by poor connections, incorrect signal levels, or marginal timing.

- ✔ Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.
- ✔ Check that the analysis probe cables and logic analyzer cables have not been physically damaged or kinked.
- ✔ Use an oscilloscope to check the signal integrity of the data lines.

Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See *Capacitive Loading* in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

The processor fetches from data memory during cache line fills. The “false” trigger may be part of a cache line fill from an instruction in the same cache line.

Trigger not seen

Only one address of the cache line fill is placed on the address bus. The other addresses are implied. Use “don’t care” terms in the trigger to capture any of the cache line addresses.

No activity on activity indicators

- ✔ Check for loose cables, board connections, and analysis probe connections.
- ✔ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ✔ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ✔ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Agilent Technologies Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

✔ Verify the values of the termination resistors on the target system.

Download the latest processor data sheet and verify that the values of the termination resistors meet the specifications.

✔ Ensure that you are following the correct power-on sequence for the analysis probe and target system.

1. Power up the analyzer and analysis probe.
2. Power up the target system.

If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

✔ Verify that the microprocessor and the interposer are securely inserted into their respective sockets.

✔ Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.

✔ Remove any extra sockets (pin protectors) which may have been added.

Erratic trace measurements

- ✔ Do a full reset of the target system before beginning the measurement.
- ✔ Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.

  See *Capacitive loading* in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.
- ✔ Ensure that you have sufficient cooling for the microprocessor.

  Ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probe add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design.

- ✔ Remove as many pin protectors, extenders, and adapters as possible.

Data bus is missing

If you do not see any activity on the data bus, it is possible that one or more strobe signals are missing. The strobes may be viewed with the Timing mode configuration. Data is presented in 16-bit slices with the _1 phase being the P strobe, and the _2 phase being the N strobe. See page 91 for more information on how the strobes relate to the data phases.

Analysis probe shuts down

If the analysis probe shuts down after 15-30 minutes of operation, then begins running again, it may be experiencing a thermal shutdown.

- ✔ Check that there is at least 5 cm (2 inches) of space in front of all ventilation holes. See “Bench Space for the Analysis Probe" on page 22.
- ✔ Check that nearby equipment is not heating the analysis probe beyond its recommended temperature range. See “Environmental Characteristics (Operating)" on page 90.
- ✔ If the analysis probe still shuts down, or if you do not hear fans running inside the analysis probe, contact Agilent Technologies.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set an oscilloscope module to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

✔ Adjust the skew in the Intermodule menu.

You may be able to specify a skew value that enables the event to be captured.

✔ Change the trigger specification for modules upstream of the one with the problem.

If you are using a logic analyzer to trigger an oscilloscope module, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Analysis Probe Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

"Measurement Initialization Error"

This error occurs when the cables between the logic analyzer cards are installed incorrectly.

Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.

See also the *Agilent Logic Analysis Systems Installation Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

✔ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

Chapter , "," beginning on page 49, describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

✔ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system frame. Ensure that the cards are firmly seated.

- ✔ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ✔ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- ✔ When analyzing microprocessors that fetch only from word-aligned addresses, ensure that the trigger condition is set to look for an opcode fetch at an address corresponding to a word boundary.

9
Hardware Reference

This chapter includes additional reference information including the specifications and characteristics of the analysis probe, as well as signal mapping tables.

Analysis probe—operating characteristics

The following operating characteristics are not specifications,

Table 1 Operating Characteristics

Operating Characteristics	
Microprocessor Supported	Intel® Xeon™ Processor Family
Socket Supported	603- or 604-pin lever-actuated socket
Clock Frequency	200 MHz maximum (BCLK)
Logic Analyzers Supported	Agilent 16753/4/5/6A logic analyzers in an Agilent 16700-series logic analysis system. (See page 43 for supported configurations.)
Analysis Probe Cable Length	Approximately 4 feet

Table 2 Inputs and Outputs

Inputs and Outputs	
To interposer	Intel® Xeon™ Processor Family processor
Between interposer and analysis probe	The Agilent E8048A interposer must be connected only to the cables from an Agilent E8047A analysis probe.
From analysis probe	High-density connectors for an Agilent 16700-series logic analysis system.

Table 3 Electrical Characteristics

Electrical Characteristics	
Power Requirements	115/230 Vac +/- 20%, 48-66Hz, 350W power supply is built into the analysis probe. Line selection is autoranging. CAT II (Line voltage in appliance and to wall outlet) Pollution degree 2
Signal Line Loading	GTL+ signals

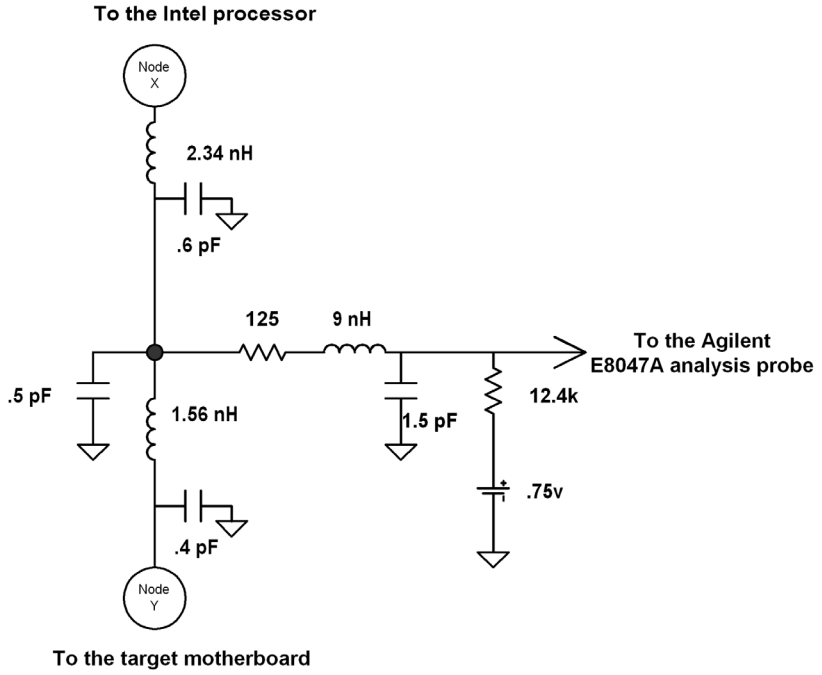


Table 4 Environmental Characteristics (Operating)

Environmental Characteristics (Operating)	
Temperature	20° to + 30° C (+68° to +86° F)
Altitude	4,600 m (15,000 ft)
Humidity	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

Signal-to-connector mapping

The following table defines the logic analyzer bit assignments.

Key

Signal Name of the signal coming from the analysis probe into the logic analysis system.

P**hase** Due to the source synchrounous nature of the bus, data captured by the logic analyzer in four chunks of 64-bit data. In a four-chunk data transfer, the analysis probe maps the four phases to two separate sets of logic analyzer pins.

Phase	BCLK	Strobe	Edge	Mapped to
1	0	P[3:0]	1st falling edge	LA Card A
2	0	N[3:0]	1st falling edge	LA Card B
3	1	P[3:0]	2nd falling edge	LA Card A
4	1	N[3:0]	2nd falling edge	LA Card B

For address signals, each of the two phases is mapped to a separate set of logic analyzer pins:.

Phase	Address strobe	Mapped to
1	falling edge	LA Card D
2	rising edge	LA Card E

Pod-Bit The logic analyzer pod containing the signal and the bit number of the particular pin on the pod. For some signals, the signal mappings are different in state and timing modes.

Label Name of the signal coming from the analysis probe into the logic analysis system, as displayed in the Format window or in a Listing window. Upper-case signal names generally correspond to signals from the processor. Lower-case signal names are generally signals generated by the analysis probe to allow the inverse assembler to properly decode bus activity.

Data signals

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
DBI3#	1,3	A4-16	A4-8	DBI1_4#	A4-16 = Clock M of LA card A
D63#	1,3	A4-15	A4-11	D63-32_1	
D62#	1,3	A4-14	A4-12	D63-32_1	
D61#	1,3	A4-13	A4-13	D63-32_1	
D60#	1,3	A4-12	A4-14	D63-32_1	
D59#	1,3	A4-11	A4-15	D63-32_1	
D58#	1,3	A4-10	A4-6	D63-32_1	
D57#	1,3	A4-9	A4-7	D63-32_1	
D56#	1,3	A4-8	A4-16	D63-32_1	
D55#	1,3	A4-7	A4-9	D63-32_1	
D54#	1,3	A4-6	A4-10	D63-32_1	
D53#	1,3	A4-5	A4-0	D63-32_1	
D52#	1,3	A4-4	A4-1	D63-32_1	
D51#	1,3	A4-3	A4-2	D63-32_1	
D50#	1,3	A4-2	A4-3	D63-32_1	
D49#	1,3	A4-1	A4-4	D63-32_1	
D48#	1,3	A4-0	A4-5	D63-32_1	
DBI2#	1,3	A3-16	A3-16	DBI1_3#	A3-16 = Clock L of LA card A
D47#	1,3	A3-15	A3-15	D63-32_1	
D46#	1,3	A3-14	A3-14	D63-32_1	
D45#	1,3	A3-13	A3-13	D63-32_1	
D44#	1,3	A3-12	A3-12	D63-32_1	
D43#	1,3	A3-11	A3-11	D63-32_1	
D42#	1,3	A3-10	A3-10	D63-32_1	
D41#	1,3	A3-9	A3-9	D63-32_1	
D40#	1,3	A3-8	A3-8	D63-32_1	
D39#	1,3	A3-7	A3-7	D63-32_1	
D38#	1,3	A3-6	A3-6	D63-32_1	
D37#	1,3	A3-5	A3-5	D63-32_1	
D36#	1,3	A3-4	A3-4	D63-32_1	
D35#	1,3	A3-3	A3-3	D63-32_1	
D34#	1,3	A3-2	A3-2	D63-32_1	
D33#	1,3	A3-1	A3-1	D63-32_1	
D32#	1,3	A3-0	A3-0	D63-32_1	

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
DBI1#	1,3	A2-16	A2-16	DBI1_2#	A2-16 = Clock K of LA card A
D31#	1,3	A2-15	A2-15	D31-00_1	
D30#	1,3	A2-14	A2-14	D31-00_1	
D29#	1,3	A2-13	A2-13	D31-00_1	
D28#	1,3	A2-12	A2-12	D31-00_1	
D27#	1,3	A2-11	A2-11	D31-00_1	
D26#	1,3	A2-10	A2-10	D31-00_1	
D25#	1,3	A2-9	A2-9	D31-00_1	
D24#	1,3	A2-8	A2-8	D31-00_1	
D23#	1,3	A2-7	A2-7	D31-00_1	
D22#	1,3	A2-6	A2-6	D31-00_1	
D21#	1,3	A2-5	A2-5	D31-00_1	
D20#	1,3	A2-4	A2-4	D31-00_1	
D19#	1,3	A2-3	A2-3	D31-00_1	
D18#	1,3	A2-2	A2-2	D31-00_1	
D17#	1,3	A2-1	A2-1	D31-00_1	
D16#	1,3	A2-0	A2-0	D31-00_1	
DBI0#	1,3	A1-16	A1-16	DBI1_1#	A1-16 = Clock J of LA card A
D15#	1,3	A1-15	A1-15	D31-00_1	
D14#	1,3	A1-14	A1-14	D31-00_1	
D13#	1,3	A1-13	A1-13	D31-00_1	
D12#	1,3	A1-12	A1-12	D31-00_1	
D11#	1,3	A1-11	A1-11	D31-00_1	
D10#	1,3	A1-10	A1-10	D31-00_1	
D9#	1,3	A1-9	A1-9	D31-00_1	
D8#	1,3	A1-8	A1-8	D31-00_1	
D7#	1,3	A1-7	A1-7	D31-00_1	
D6#	1,3	A1-6	A1-6	D31-00_1	
D5#	1,3	A1-5	A1-5	D31-00_1	
D4#	1,3	A1-4	A1-4	D31-00_1	
D3#	1,3	A1-3	A1-3	D31-00_1	
D2#	1,3	A1-2	A1-2	D31-00_1	
D1#	1,3	A1-1	A1-1	D31-00_1	
D0#	1,3	A1-0	A1-0	D31-00_1	

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
DBI3#	2,4	B4-16		DBI2_4#	Clock M of LA card B
D63#	2,4	B4-15		D63-32_2	
D62#	2,4	B4-14		D63-32_2	
D61#	2,4	B4-13		D63-32_2	
D60#	2,4	B4-12		D63-32_2	
D59#	2,4	B4-11		D63-32_2	
D58#	2,4	B4-10		D63-32_2	
D57#	2,4	B4-9		D63-32_2	
D56#	2,4	B4-8		D63-32_2	
D55#	2,4	B4-7		D63-32_2	
D54#	2,4	B4-6		D63-32_2	
D53#	2,4	B4-5		D63-32_2	
D52#	2,4	B4-4		D63-32_2	
D51#	2,4	B4-3		D63-32_2	
D50#	2,4	B4-2		D63-32_2	
D49#	2,4	B4-1		D63-32_2	
D48#	2,4	B4-0		D63-32_2	
DBI2#	2,4	B3-16		DBI2_3#	Clock L of LA card B
D47#	2,4	B3-15		D63-32_2	
D46#	2,4	B3-14		D63-32_2	
D45#	2,4	B3-13		D63-32_2	
D44#	2,4	B3-12		D63-32_2	
D43#	2,4	B3-11		D63-32_2	
D42#	2,4	B3-10		D63-32_2	
D41#	2,4	B3-9		D63-32_2	
D40#	2,4	B3-8		D63-32_2	
D39#	2,4	B3-7		D63-32_2	
D38#	2,4	B3-6		D63-32_2	
D37#	2,4	B3-5		D63-32_2	
D36#	2,4	B3-4		D63-32_2	
D35#	2,4	B3-3		D63-32_2	
D34#	2,4	B3-2		D63-32_2	
D33#	2,4	B3-1		D63-32_2	
D32#	2,4	B3-0		D63-32_2	

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
DBI1#	2,4	B2-16		DBI2_2#	Clock K of LA card B
D31#	2,4	B2-15		D31-00_2	
D30#	2,4	B2-14		D31-00_2	
D29#	2,4	B2-13		D31-00_2	
D28#	2,4	B2-12		D31-00_2	
D27#	2,4	B2-11		D31-00_2	
D26#	2,4	B2-10		D31-00_2	
D25#	2,4	B2-9		D31-00_2	
D24#	2,4	B2-8		D31-00_2	
D23#	2,4	B2-7		D31-00_2	
D22#	2,4	B2-6		D31-00_2	
D21#	2,4	B2-5		D31-00_2	
D20#	2,4	B2-4		D31-00_2	
D19#	2,4	B2-3		D31-00_2	
D18#	2,4	B2-2		D31-00_2	
D17#	2,4	B2-1		D31-00_2	
D16#	2,4	B2-0		D31-00_2	
DBI0#	2,4	B1-16		DBI2_1#	Clock J of LA card B
D15#	2,4	B1-15		D31-00_2	
D14#	2,4	B1-14		D31-00_2	
D13#	2,4	B1-13		D31-00_2	
D12#	2,4	B1-12		D31-00_2	
D11#	2,4	B1-11		D31-00_2	
D10#	2,4	B1-10		D31-00_2	
D9#	2,4	B1-9		D31-00_2	
D8#	2,4	B1-8		D31-00_2	
D7#	2,4	B1-7		D31-00_2	
D6#	2,4	B1-6		D31-00_2	
D5#	2,4	B1-5		D31-00_2	
D4#	2,4	B1-4		D31-00_2	
D3#	2,4	B1-3		D31-00_2	
D2#	2,4	B1-2		D31-00_2	
D1#	2,4	B1-1		D31-00_2	
D0#	2,4	B1-0		D31-00_2	

Address Signals

A2, A1, A0 are set to logic 0 on the analysis probe to aid in triggering on address.

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
A35#	1	D3-3	D3-3	A35-32_1	
A34#	1	D3-2	D3-2	A35-32_1	
A33#	1	D3-1	D3-1	A35-32_1	
A32#	1	D3-0	D3-0	A35-32_1	
A31#	1	D2-15	D2-14	A31-00_1	
A30#	1	D2-14	D2-13	A31-00_1	
A29#	1	D2-13	D2-12	A31-00_1	
A28#	1	D2-12	D2-11	A31-00_1	
A27#	1	D2-11	D2-10	A31-00_1	
A26#	1	D2-10	D2-9	A31-00_1	
A25#	1	D2-9	D2-8	A31-00_1	
A24#	1	D2-8	D2-15	A31-00_1	
A23#	1	D2-7	D2-7	A31-00_1	
A22#	1	D2-6	D2-6	A31-00_1	
A21#	1	D2-5	D2-5	A31-00_1	
A20#	1	D2-4	D2-4	A31-00_1	
A19#	1	D2-3	D2-3	A31-00_1	
A18#	1	D2-2	D2-2	A31-00_1	
A17#	1	D2-1	D2-1	A31-00_1	
A16#	1	D2-0	D2-0	A31-00_1	
A15#	1	D1-15	D1-14	A31-00_1	
A14#	1	D1-14	D1-13	A31-00_1	
A13#	1	D1-13	D1-12	A31-00_1	
A12#	1	D1-12	D1-11	A31-00_1	
A11#	1	D1-11	D1-10	A31-00_1	
A10#	1	D1-10	D1-9	A31-00_1	
A9#	1	D1-9	D1-8	A31-00_1	
A8#	1	D1-8	D1-15	A31-00_1	
A7#	1	D1-7	D1-7	A31-00_1	
A6#	1	D1-6	D1-6	A31-00_1	
A5#	1	D1-5	D1-5	A31-00_1	

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
A4#	1	D1-4	D1-4	A31-00_1	
A3#	1	D1-3	D1-3	A31-00_1	
	1	D1-2	D1-2	A31-00_1	A2 set to 0, generated by analysis probe
	1	D1-1	D1-1	A31-00_1	State: A1 set to 0, generated by analysis probe; Timing: D1-1 is AGTB1
	1	D1-0	D1-0	A31-00_1	State: A0 set to 0, generated by analysis probe; Timing: D1-0 is AGTB0
A35#	2	E3-3		A35-32_2	
A34#	2	E3-2		A35-32_2	
A33#	2	E3-1		A35-32_2	
A32#	2	E3-0		A35-32_2	
A31#	2	E2-15		A31-00_2	
A30#	2	E2-14		A31-00_2	
A29#	2	E2-13		A31-00_2	
A28#	2	E2-12		A31-00_2	
A27#	2	E2-11		A31-00_2	
A26#	2	E2-10		A31-00_2	
A25#	2	E2-9		A31-00_2	
A24#	2	E2-8		A31-00_2	
A23#	2	E2-7		A31-00_2	
A22#	2	E2-6		A31-00_2	
A21#	2	E2-5		A31-00_2	
A20#	2	E2-4		A31-00_2	
A19#	2	E2-3		A31-00_2	
A18#	2	E2-2		A31-00_2	
A17#	2	E2-1		A31-00_2	
A16#	2	E2-0		A31-00_2	
A15#	2	E1-15		A31-00_2	
A14#	2	E1-14		A31-00_2	
A13#	2	E1-13		A31-00_2	
A12#	2	E1-12		A31-00_2	
A11#	2	E1-11		A31-00_2	
A10#	2	E1-10		A31-00_2	
A9#	2	E1-9		A31-00_2	
A8#	2	E1-8		A31-00_2	
A7#	2	E1-7		A31-00_2	

Signal	Phase	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
A6#	2	E1-6		A31-00_2	
A5#	2	E1-5		A31-00_2	
A4#	2	E1-4		A31-00_2	
A3#	2	E1-3		A31-00_2	
	2	E1-2		A31-00_2	A2 set to 0, generated by analysis probe
	2	E1-1		A31-00_2	A1 set to 0, generated by analysis probe
	2	E1-0		A31-00_2	A0 set to 0, generated by analysis probe

Control Signals

Do not change the setup/hold configuration. For most control signals, setup time is configured as 3.500 ns and hold time as -1.000 ns. The signals generated by the analysis probe use setup=2.500 ns and hold=0.

Signal	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
The following control signals are captured on the processor front side bus:				
A20M	D1-16	D1-16	A20M	Clock J of LA card D
ADS#	C2-7	C2-7	ADS#	
AP0#	D4-14	D4-12	AP# (Label Bit 0)	
AP1#	D4-15	D4-13	AP# (Label Bit 1)	
BCLK	C1-16	C1-16	BCLK	Clock J of LA card C
BINIT#	C2-0	C2-0	BINIT#	
BNR#	D3-12	D3-12	BNR#	
BPM0#	D4-4	D4-4	BPM# (Label Bit 0)	
BPM1#	D4-5	D4-5	BPM# (Label Bit 1)	
BPM2#	D4-6	D4-6	BPM# (Label Bit 2)	
BPM3#	D4-7	D4-7	BPM# (Label Bit 3)	
BPM4#	D4-8	D4-15	BPM# (Label Bit 4)	
BPM5#	D4-9	D4-8	BPM# (Label Bit 5)	
BPRI#	D3-13	D3-13	BPRI#	
DBSY#	C2-3	C2-3	DBSY#	
			DSTBS (Label Bit 0)	
			DSTBS (Label Bit 1)	
			DSTBS (Label Bit 2)	
			DSTBS (Label Bit 3)	
			DSTBS (Label Bit 4)	
			DSTBS (Label Bit 5)	
			DSTBS (Label Bit 6)	
			DSTBS (Label Bit 7)	
DEFER#	D3-14	D3-16	DEFER#	Clock L of LA card D
DP0#	D4-0	D4-0	DP0#	
DP1#	D4-1	D4-1	DP1#	
DP2#	D4-2	D4-2	DP2#	
DP3#	D4-3	D4-3	DP3#	
DRDY#	C2-4	C2-4	DRDY#	

Signal	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
FERR#	E4-16	E4-16	FERR#	Clock M of LA card E
HIT#	C2-9	C2-9	HIT#	
HITM#	C2-10	C2-10	HITM#	
IERR#	E4-15	E4-15	IERR#	
IGNNE#	E3-12	E3-12	IGNNE#	
INIT#	E4-8	E4-8	INIT#	
LINT0/INTR	D3-16	D4-14	LINT0/INTR	D3-16 = Clock L of LA Card D
LINT1/NMI	D4-16	D4-16	LINT1/NMI	D4-16 = Clock M of LA Card D
LOCK#	D2-16	D2-16	LOCK#	Clock K of LA card D
MCERR#	C2-1	C2-1	MCERR#	
PROCHOT#	E4-11	E4-11	PROCHOT#	
PWRGOOD	E4-12	E4-12	PWRGOOD	
REQ0	D3-8	D3-15	REQ (Label Bit 0)	
REQ1	D3-9	D3-8	REQ (Label Bit 1)	
REQ2	D3-10	D3-9	REQ (Label Bit 2)	
REQ3	D3-11	D3-10	REQ (Label Bit 3)	
REQ4	D3-15	D3-11	REQ (Label Bit 4)	
RESET#	C2-11	C2-11	RESET#	
RS0#	C2-8	C2-8	RS0#	
RS1#	C2-5	C2-5	RS1#	
RS2#	C2-6	C2-6	RS2#	
RSP#	E4-9	E4-9	RSP#	
SLP#	E4-6	E4-6	SLP	
SMI#	E3-14	E3-14	SMI#	
STPCLK#	E4-10	E4-10	STPCLK#	
THRMTRIP#	E3-16	E3-16	THRMTRIP#	Clock L of LA card E
TRDY#	C2-2	C2-2	TRDY#	
TRST#	E2-16	E2-16	TRST#	Clock K of LA card E
VID0	-	E4-0		
VID1	-	E4-1		
VID2	-	E4-2		
VID3	-	E4-3		
VID4	-	E4-4		
VID5	-	E4-5		
VIDPWRGOOD	E4-7	E4-7		

The following signals are generated by the analysis probe for use by the software only:

Signal	Pod-Bit (State)	Pod-Bit (Timing)	Label	Description
	C1-8		cqual	Used to identify inactive states
	C1-10		ppMode	Tells SW that analysis probe is in compact or expanded mode
	D3[15] D3[11:8] E3[10:8] C2[7]		tranTy	

10
General-Purpose ASCII (GPA) Symbol File Format

The General-purpose ASCII format allows you to create symbol files without the help of a compiler or assembler.

General-purpose ASCII (GPA) format files are loaded into a logic analyzer just like other object files, but they are usually created differently.

If your compiler does not include symbol information in the output, or if you want to define a symbol not in the object file, you can create an ASCII format symbol file.

Typically, ASCII format symbol files are created using text processing tools to convert compiler or linker map file output that has symbolic information into the proper format.

You can typically get symbol table information from a linker map file to create a General-Purpose ASCII (GPA) symbol file.

Various kinds of symbols are defined in different records in the GPA file. Record headers are enclosed in square brackets; for example, [VARIABLES]. For a summary of GPA file records and associated symbol definition syntax, refer to the “GPA Record Format Summary” that follows.

Each entry in the symbol file must consist of a symbol name followed by an address or address range.

While symbol names can be very long, the logic analyzer only uses the first 16 characters.

The address or address range corresponding to a given symbol appears as a hexadecimal number. The address or address range must immediately follow the symbol name, appear on the

same line, and be separated from the symbol name by one or more blank spaces or tabs. Ensure that address ranges are in the following format:

```
beginning address..ending address
```

Example

```
main    00001000..00001009
test    00001010..0000101F
var1    00001E22            #this is a variable
```

This example defines two symbols that correspond to address ranges and one point symbol that corresponds to a single address.

For more detailed descriptions of GPA file records and associated symbol definition syntax, refer to these topics that follow:

- SECTIONS
- FUNCTIONS
- VARIABLES
- SOURCE LINES
- START ADDRESS
- Comments

GPA Record Format Summary

```
[SECTIONS]
section_name start..end attribute

[FUNCTIONS]
func_name start..end

[VARIABLES]
var_name start [size]
var_name start..end

[SOURCE LINES]
File: file_name
line# address

[START ADDRESS]
address

#Comments
```

If no record header is specified, [VARIABLES] is assumed. Lines without a preceding header are assumed to be symbol definitions in one of the VARIABLES formats.

Example

This is an example GPA file that contains several different kinds of records:

```
[SECTIONS]
prog     00001000..0000101F
data     40002000..40009FFF
common   FFFF0000..FFFF1000

[FUNCTIONS]
main     00001000..00001009
test     00001010..0000101F

[VARIABLES]
total    40002000  4
value    40008000  4
```

```
[SOURCE LINES]
File: main.c
10       00001000
11       00001002
14       0000100A
22       0000101E

File: test.c
 5       00001010
 7       00001012
11       0000101A
```

SECTIONS

```
[SECTIONS]
section_name  start..end  attribute
```

Use SECTIONS to define symbols for regions of memory, such as sections, segments, or classes.

`section_name` A symbol representing the name of the section.

`start` The first address of the section, in hexadecimal.

`end` The last address of the section, in hexadecimal.

`attribute` This is optional, and may be one of the following:

- NORMAL (default)—The section is a normal, relocatable section, such as code or data.
- NONRELOC—The section contains variables or code that cannot be relocated; this is an absolute segment.

NOTE

Define sections first

To enable section relocation, section definitions must appear before any other definitions in the file.

Example

```
[SECTIONS]
prog           00001000..00001FFF
data           00002000..00003FFF
display_io     00008000..0000801F  NONRELOC
```

If you use section definitions in a GPA symbol file, any subsequent function or variable definitions must be within the address ranges of one of the defined sections. Functions and variables that are not within the range are ignored.

FUNCTIONS

```
[FUNCTIONS]
func_name start..end
```

Use FUNCTIONS to define symbols for program functions, procedures, or subroutines.

`func_name` A symbol representing the function name.

`start` The first address of the function, in hexadecimal.

`end` The last address of the function, in hexadecimal.

Example

```
[FUNCTIONS]
main     00001000..00001009
test     00001010..0000101F
```

VARIABLES

```
[VARIABLES]
var_name   start [size]
var_name   start..end
```

You can specify symbols for variables either by using the address of the variable, the address and the size of the variable, or a range of addresses occupied by the variable. If you specify only the address of a variable, the size is assumed to be one byte.

`var_name` A symbol representing the variable name.

`start` The first address of the variable, in hexadecimal.

`end` The last address of the variable, in hexadecimal.

`size` This is optional, and indicates the size of the variable, in bytes, in decimal.

Example

```
[VARIABLES]
subtotal     40002000   4
total        40002004   4
data_array   40003000..4000302F
status_char  40002345
```

SOURCE LINES

```
[SOURCE LINES]
File: file_name
line#  address
```

Use SOURCE LINES to associate addresses with lines in your source files.

`file_name` The name of a file.

`line#` The number of a line in the file, in decimal.

`address` The address of the source line, in hexadecimal.

Example

```
[SOURCE LINES]
File: main.c
10       00001000
11       00001002
14       0000100A
22       0000101E
```

START ADDRESS

```
[START ADDRESS]
address
```

`address` The address of the program entry point, in hexadecimal.

Example

```
[START ADDRESS]
00001000
```

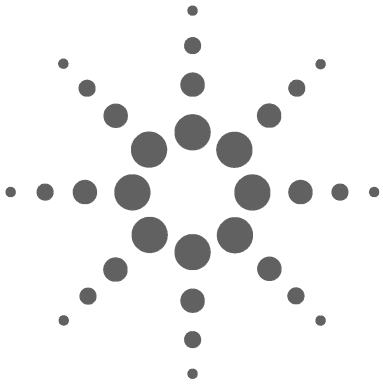
Comments

```
#comment text
```

Use the # character to include comments in a file. Any text following the # character is ignored. You can put comments on a line alone or on the same line following a symbol entry.

Example

```
#This is a comment.
```



11
Service Guide

To return a part to Agilent Technologies for service

1. Follow the procedures in the “Troubleshooting...” chapters to make sure that the problem is caused by a hardware failure, not by configuration or cabling problems.
2. In the U.S., call 1-877-4Agilent (1-877-424-4536). Outside the U.S., call your nearest Agilent sales office. Ask them for the address of the nearest Agilent service center.
3. Package the part and send it to the Agilent service center.

   Keep any parts which you know are working.
4. When the part has been replaced, it will be sent back to you.

The unit returned to you will have the same serial number as the unit you sent to Agilent.

The Agilent service center can also troubleshoot the hardware and replace the failed part. To do this, send your entire measurement system to the service center, including the logic analysis system and cables.

In some parts of the world, on-site repair service is available. Ask an Agilent sales or service representative for details.

To get replacement parts

The repair strategy for this product is board replacement. However, the following tables list some mechanical parts that may be replaced if they are damaged or lost. Contact your Agilent Technologies Sales Office for further information.

For some parts, exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the “Exchange Assembly” program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Agilent Part Number	Description
E8047-69001	Analysis Probe Assembly
E8048-60004	Interposer
E8048-68702	Accessory kit

Part numbers are subject to change without notice.

12
Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the analysis probe requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source. Do not attempt to clean the interposer.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product..

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Agilent Technologies

DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

Manufacturer's Name:	Agilent Technologies, Inc.
Manufacturer's Address:	1900 Garden of the Gods Road Colorado Springs, Colorado 80907 U.S.A.

Declares, that the product

Product Name:	Analysis Probes for the Intel Pentium 4 Processor and Intel Xeon Processor Family
Model Number:	E8045A, E8046A, E8047A and E8048A
Product Options:	This declaration covers all options of the above product(s).

Conforms with the following product stardands:

EMC	**Standard**	**Limit**
	IEC 61326-2:2002 / EN 61326-1:1997	
	CCISPR 11:1997+A1:1999/EN 55011:1991	Group 1 Class A[1]
	IEC 61000-4-2:1995+A1:1998+A2:2000/EN 61000-4-2:1995	4kV CD, 8kV AD
	IEC 61000-4-3:1995+A1:1998+A2:2000/EN 61000-4-3:1995	3V/m, 80-1000 MHz
	IEC 61000-4-4:1995+A1:2000+A2:2001/EN 61000-4-4:1995	0.5kV signal lines, 1kV power lines
	IEC 61000-4-5:1995/EN 61000-4-5:1995	0.5kV line-line, 1kV line-ground
	IEC 61000-4-6:1996+A1:2000/EN 61000-4-6:1996	3V, 0.15-80 MHz
	IEC 61000-4-11:1994/EN 61000-4-11:1994	1 cycle, 100%
	Canada: ICES/NMB-001:1998	
	Australia/New Zealand: AS/NZS 2064.1	
Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995	
	Canada: CSA C22.2 No. 1010.1:1992	

Additional Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE-marking accordingly (European Union).

[1] The product was tested in a typical configuration with Agilent Technologies test systems.

Date: 2002-9-18

Ken Wyatt

Name

Ken Wyatt / Product Regulations Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.

Product Regulations

EMC	Performance Criteria[1]
IEC 61326-2:2002 / EN 61326-1:1997 CISPR 11:1997+A1:1999 / EN 55011:1991- Group 1 Class A	
IEC 61000-4-2:1995+A1:1998+A2:2000 / EN 61000-4-2:1995 (ESD 4kV CD, 8kV AD)	C
IEC 61000-4-3:1995+A1:1998+A2:2000 / EN 61000-4-3:1995 (3V/m 80% AM)	C
IEC 61000-4-4:1995+A1:2000+A2:2001 / EN 61000-4-4:1995 (EFT 0.5kV line-line, 1kV line-earth)	C
IEC 61000-4-5:1995 / EN 61000-4-5:1995 (Surge 0.5kV line-line, 1kV line-earth)	A
IEC 61000-4-6:1996+A1:2000 / EN 61000-4-6:1996 (3V 80% AM, power line)	C
IEC 61000-4-11:1994 / EN 61000-4-11:1994 (Dips 1 cycle, 100%)	A

Safety IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995
Canada: CSA C22.2 No. 1010.1:1992
USA: UL 3111-1:1994 {optional}

Additional Information

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

[1] Performance Criteria:
- A Pass - Normal operation, no effect.
- B Pass - Temporary degradation, self recoverable.
- C Pass - Temporary degradation, operator intervention required.
- D Fail - Not recoverable, component damage.

Note:
IEC 61000-4-6 is not applicable to this product.

Sound Pressure Level Less than 60 dBA

Regulatory Information for Canada

ICES/NMB-001:1998

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est confomre à la norme NMB-001 du Canada.

Regulatory Information for Australia/New Zealand

This ISM device complies with Australian/New Zealand AS/NZS 2064.1

N10149

Glossary

Analysis Probe A probing solution connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer. Also known as a “preprocessor” or an "LAI."

Deskewing To cancel or nullify the effects of differences between two different internal delay paths for a signal. Deskewing is normally done by routing a single test signal to the inputs of two different modules, then adjusting the Intermodule Skew so that both modules recognize the signal at the same time.

Extender A part whose only function is to provide connections from one location to another. One or more extenders might be stacked to raise a probe above a target microprocessor to avoid mechanical contact with other components installed close to the target microprocessor. Sometimes called a "connector board."

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High-Density Termination Adapter Cable Same as a High-Density Adapter Cable, except it has a termination in the Mictor connector.

Intermodule Bus The intermodule bus (IMB) is a bus in the frame that allows the measurement modules to communicate with each other. Using the IMB, you can set up one instrument to *arm* another. Data acquired by instruments using the IMB is time-correlated.

Intermodule Intermodule is a term used when multiple instrument tools are connected together for the purpose of one instrument arming another. In such a configuration, an arming tree is developed and the group run function is designated to start all instrument tools. Multiple instrument configurations are done in the Intermodule window.

Interposer A device which is placed between the the microprocessor and its socket to bring the signals out to a more accessible location.

Inverse Assembler Software that displays captured bus activity as assembly language mnemonics. In addition, inverse assemblers may show execution history or decode control busses.

Label Labels are used to group and identify logic analyzer channels. A label consists of a name and an associated bit or group of bits.

LAI Logic Analyzer Interface, see *Analysis Probe*.

LIF Socket Low insertion force socket.

Machine Some logic analyzers allow you to set up two measurements at the same time. Each measurement is handled by a different machine. This is represented in the Workspace window by two icons, differentiated by a *1* and a *2* in the upper right-hand corner of the icon. Logic analyzer resources such as pods and trigger terms cannot be shared by the machines. Multiple cards in a logic analysis system may be connected together (with cables) as a single machine; if they are not connected together, they operate as independent machines.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an Agilent 16500, Agilent 1660-series, or Agilent 16600A/700A-series mainframe.

Markers Markers are the green and yellow lines in the display that are labeled *x*, *o*, *G1*, and *G2*. Use them to measure time intervals or sample intervals. Markers are assigned to patterns in order to find patterns or track sequences of states in the data. The x and o markers are local to the immediate display, while G1 and G2 are global between time correlated displays.

Master Card In a module, the master card controls the data acquisition or output. The logic analysis system references the module by the slot in which the master card is plugged. For example, a 5-card Agilent Technologies 16555D would be referred to as Slot C: machine because the master card is in slot C of the mainframe. The other cards of the module are called expansion cards.

Module An instrument that uses a single timebase in its operation. Modules can have from one to five cards functioning as a single instrument. When a module has more than one card, system window will show the instrument icon in the slot of the *master card.*

Preprocessor See Analysis Probe.

Setup Assistant A software program that guides a user through the process of connecting and configuring a logic analyzer to make measurements on a specific microprocessor.

Skew Skew is the difference in channel delays between measurement channels. Typically, skew between modules is caused by differences in designs of measurement channels, and differences in characteristics of the electronic components within those channels. You should adjust measurement modules to eliminate as much skew as possible so that it does not affect the accuracy of your measurements.

State Measurement In a state measurement, the logic analyzer is clocked by a signal from the system under test. Each time the clock signal becomes valid, the analyzer samples data from the system under test. Since the analyzer is clocked by the system, state measurements are synchronous with the test system.

Store Qualification Store qualification is only available in a state measurement, not timing measurements. Store qualification allows you to specify the type of information (all samples, no samples, or selected states) to be stored in memory. Use store qualification to prevent memory from being filled with unwanted activity such as no-ops or wait-loops. To set up store qualification, use the While storing field in a logic analyzer trigger sequence dialog.

Symbol Symbols represent patterns and ranges of values found on labeled sets of bits. Two kinds of symbols are available:
1) Object file symbols — Symbols from your source code, and symbols generated by your compiler. Object file symbols may represent global variables, functions, labels, and source line numbers.
2) User-defined symbols — Symbols you create.

Target Control Port An 8-bit, TTL port on a logic analysis system that you can use to send signals to your target system. It does not function like a pattern generator or emulation module, but more like a remote control for the target's switches.

Target System The device under test.

Timing Measurement In a timing measurement, the logic analyzer samples data at regular intervals according to a clock signal internal to the timing analyzer. Since the analyzer is clocked by a signal that is not related to the system under test, timing measurements capture traces of electrical activity over time. These measurements are *asynchronous* with the test system.

Tool Icon Tool icons that appear in the workspace are representations of the hardware and software tools selected from the toolbox. If they are placed directly over a current measurement, the tools automatically connect to that measurement. If they are placed on an open area of the main window, you must connect them to a measurement using the mouse.

Trigger Trigger is an event that occurs immediately after the instrument recognizes a match between the incoming data and the trigger specification. Once trigger occurs, the instrument completes its *acquisition*, including any store qualification that may be specified.

Trigger Sequence A trigger sequence is a sequence of events that you specify. The logic analyzer compares this sequence with the samples it is collecting to determine when to *trigger*.

Trigger Specification A set of conditions that must be true before the instrument triggers. See the printed or online documentation of your logic analyzer for details.

Workspace The workspace is the large area under the message bar and to the right of the toolbox. The workspace is where you place the different instrument, display, and analysis tools. Once in the workspace, the tool icons graphically represent a complete picture of the measurements.

ZIF Socket Zero insertion force socket.

Index

T

U

V

W